HW01-18: Closed-Loop Control of a Buck Converter

808-PowerLab NCTU HSINCHU TAIWAN

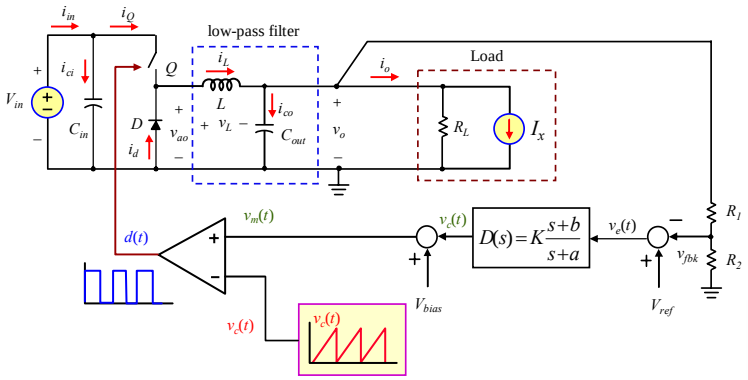

Fig. (a) Schematics of simple voltage mode buck switching regulator.

The purpose of a switching regulator is to maintain its output under load disturbances and input voltage variations. This can only be achieved via feedback control scheme. There are two basic approaches to achieve the closed-loop control of a switching converter: one is the voltage-mode control via the output feedback only; the other is current-mode control by adding an inner current control loop to regulate the inductor current. The schematics of voltage-mode buck switching regulator is illustrated in Fig. a with its circuit parameters given in HW12-04. **This homework assignment is to study the design of the loop compensator D(s) on the dynamic responses of the buck converter under load disturbances.**

HW01-18: Type of the Loop Compensator

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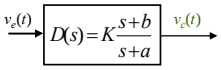
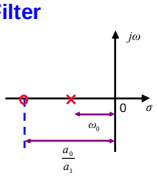


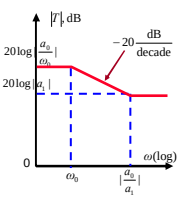
There are many types of the feedback controller, such as PID, phase-lead, 2nd-order filter, or a specifically designed frequency compensator, can be used as the loop compensator for the closed-loop voltage regulation of the buck converter. According to the given first-order compensator, design or tuning a set of the controller parameters K, a, and b to improve the dynamic response under input voltage variations and load disturbances as given in HW01-04.

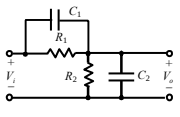
Note: A bias voltage V_{bias} is required to bias the output of the loop compensator at the middle of the carrier signal to achieve a symmetric and maximum dynamic range of the control signal.

First-Order Filter

$$T(s) = \frac{a_1 s + a_0}{s + \omega_0}$$





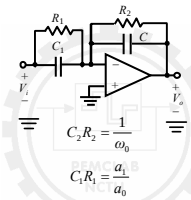


$$(C_1 + C_2)(R_1 + R_2) = \frac{1}{\omega_0}$$

$$C_1 R_1 = \frac{a_0}{a_1}$$

$$\text{dc gain} = \frac{R_2}{R_1 + R_2}$$

$$\text{HF gain} = \frac{C_1}{C_1 + C_2}$$



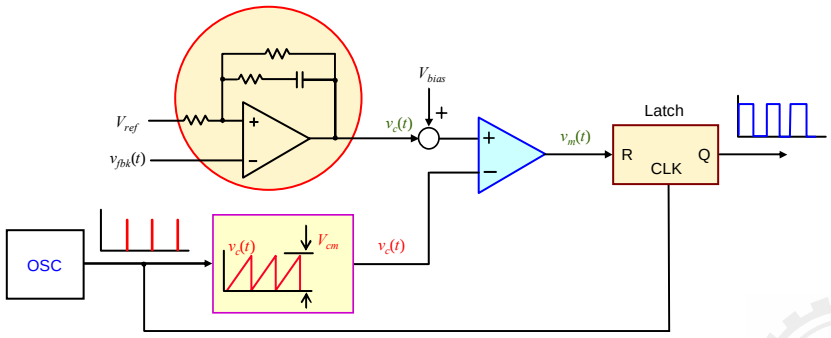
$$C_2 R_2 = \frac{1}{\omega_0}$$

$$C_1 R_1 = \frac{a_1}{a_0}$$

$$\text{dc gain} = -\frac{R_2}{R_1}$$

$$\text{HF gain} = -\frac{C_1}{C_2}$$

HW01-18: Latch to ensure a constant switching frequency



The **OSC** (oscillator) is used to generate a fixed switching frequency for the buck converter.

The **saw-tooth carrier generator** can be realized by an clock triggered integrator or by the OSC with a one-shot triggered circuit.

The **LATCH** is used prevent the switching more than once during one switching period due to sensing noises to the comparator, or a too large gain to induce high frequency oscillation, etc.

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HW01-18: Problems and Discussions

1. Make a circuit realization of the given loop compensator. You may use an ideal OP Amp to realize the designed circuit. Describe the circuit design.
2. Design or tuning the control parameters to improve the dynamic responses of the under load disturbances and input voltage variations as defined in HW01-04, operating modes from A to F. Plot the time responses with and without feedback control.
3. The input voltage is set at 10V, the PWM control duty is set at 50%, and the load is fixed at 2.5Ω, plot the frequency responses of the output impedance of the buck converter under open-loop and closed-loop control conditions.
4. Plot the loop gain of the designed buck regulator.
5. Make a discussion of the designed loop compensator according to the loop gain, output impedance, and time responses under step load current change.
6. Is there a difference by using a phase-lead or phase-lag loop compensator?

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References

Keywords: DC to DC, Buck, Boost, Flyback, Inverter, PWM, Quick-PWM, Voltage Mode, Current Mode Skip, Synchronous Rectifier

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APPLICATION NOTE 2031

DC-DC Converter Tutorial

Abstract: Switching power supplies offer higher efficiency than traditional linear power supplies. They can step-up, step-down, and invert. Some designs can isolate output voltage from the input. This article outlines the different types of switching regulators used in DC-DC conversion. It also reviews and compares the various control techniques for these converters.

Introduction

The power switch was the key to practical switching regulators. Prior to the invention of the Vertical Metal Oxide Semiconductor (VMOS) power switch, switching supplies were generally not practical.

The inductor's main function is to limit the current slew rate through the power switch. This action limits the otherwise high-peak current that would be limited by the switch resistance alone. The key advantage for using an inductor in switching regulators is that an inductor stores energy. This energy can be expressed in Joules as a function of the current by:

$$E = \frac{1}{2} * L * I^2$$

A linear regulator uses a resistive voltage drop to regulate the voltage, losing power (voltage drop times the current) in the form of heat. A switching regulator's inductor does have a voltage drop and an associated current but the current is 90 degrees out of phase with the voltage. Because of this, the energy is stored and can be recovered in the discharge phase of the switching cycle. This results in a much higher efficiency and much less heat.

What Is a Switching Regulator?

A switching regulator is a circuit that uses a power switch, an inductor, and a diode to transfer energy from input to output.

The basic components of the switching circuit can be rearranged to form a step-down (buck), step-up (boost), or an inverter (flyback). These designs are shown in **Figures 1**, **2**, **3**, and **4** respectively, where Figures 3 and 4 are the same except for the transformer and the diode polarity. Feedback and control circuitry can be carefully nested around these circuits to regulate the energy transfer and maintain a constant output within normal operating conditions.

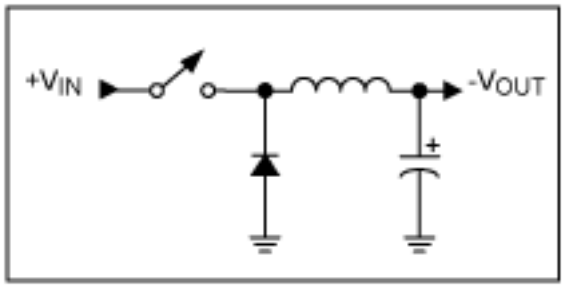

Figure 1. Buck converter topology.

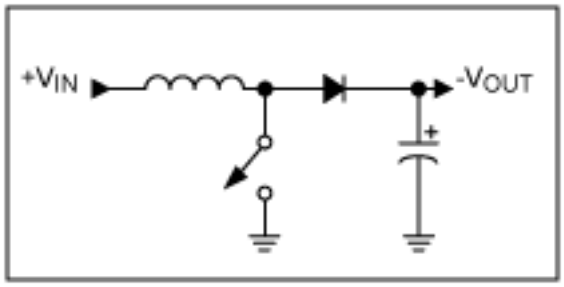

Figure 2. Simple boost converter.

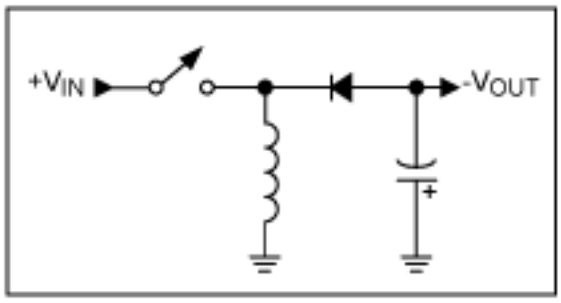

Figure 3. Inverting topology.

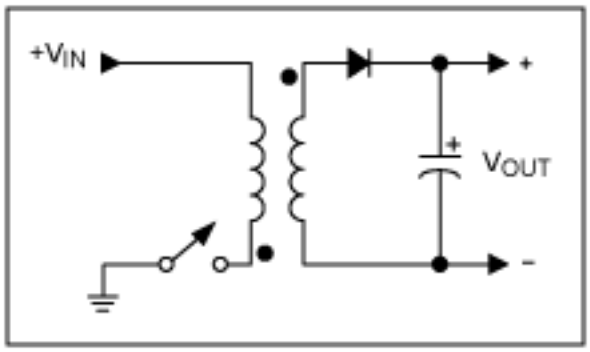

Figure 4. Transformer flyback topology.

Why Use a Switching Regulator?

Switching regulators offer three main advantages compared to a linear regulators. First, switching efficiency can be much better than linear. Second, because less energy is lost in the transfer, smaller components and less thermal management are required. Third, the energy stored by an inductor in a switching regulator can be transformed to output voltages that can be greater than the input (boost), negative (inverter), or can even be transferred through a transformer to provide electrical isolation with respect to the input (Figure 4).

Given the advantages of switching regulators, one might wonder where can linear regulators be used? Linear regulators provide lower noise and higher bandwidth; their simplicity can sometimes offer a less expensive solution.

There are, admittedly, disadvantages with switching regulators. They can be noisy and require energy management in the form of a control loop. Fortunately the solution to these control problems is found integrated in modern switching-mode controller chips.

Charge Phase

A basic boost configuration is depicted in **Figure 5**. Assuming that the switch has been open for a long time and that the voltage drop across the diode is negative, the voltage across the capacitor is equal to the input voltage. When the switch closes, the input voltage, $+V_{IN}$, is impressed across the inductor and the diode prevents the capacitor from discharging $+V_{OUT}$ to ground. Because the input voltage is DC, current through the inductor rises

linearly with time at a rate proportional to the input voltage divided by the inductance.

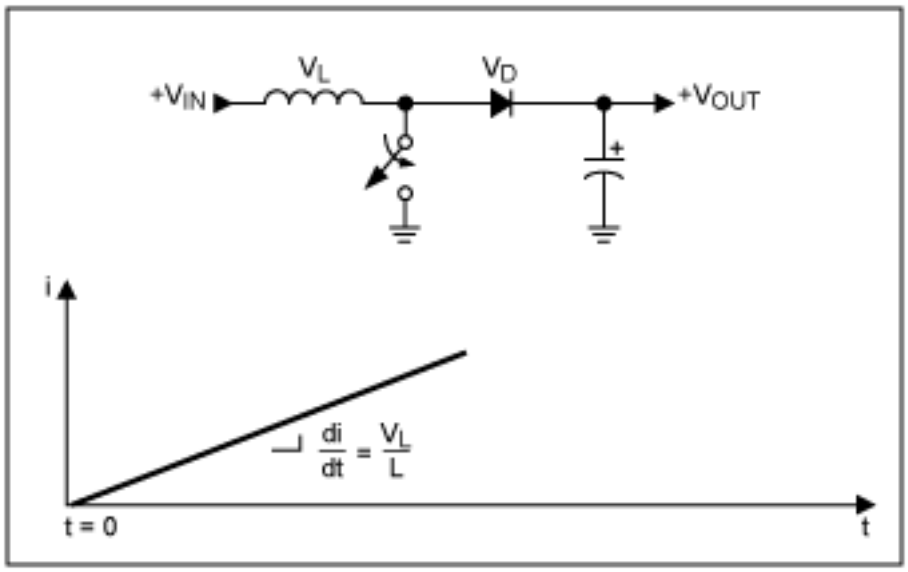

Figure 5. Charging phase: when the switch closes, current ramps up through the inductor.

Discharge Phase

Figure 6 shows the discharge phase. When the switch opens again, the inductor current continues to flow into the rectification diode to charge the output. As the output voltage rises, the slope of the current, di/dt, though the inductor reverses. The output voltage rises until equilibrium is reached or:

$V_L = L \times di/dt$

In other words, the higher the inductor voltage, the faster inductor current drops.

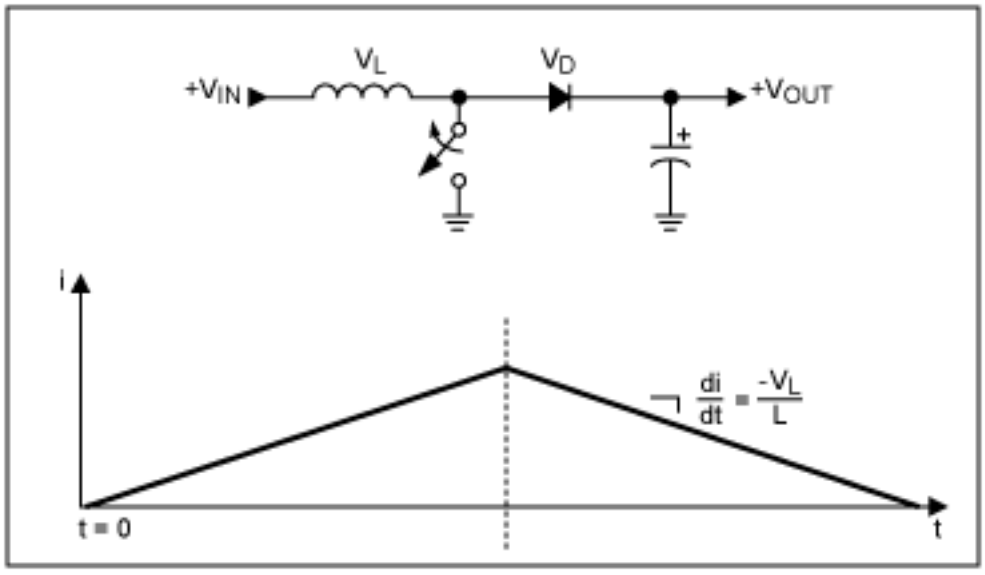

Figure 6. Discharge phase: when the switch opens, current flows to the load through the rectifying diode.

In a steady-state operating condition the average voltage across the inductor over the entire switching cycle is zero. This implies that the average current through the inductor is also in steady state. This is an important rule governing all inductor-based switching topologies. Taking this one step further, we can establish that for a given charge time, t_{ON}, and a given input voltage and with the circuit in equilibrium, there is a specific discharge time, t_{OFF}, for an output voltage. Because the average inductor voltage in steady state must equal zero, we can calculate for the boost circuit:

$V_{IN} \times t_{ON} = t_{OFF} \times V_L$

and because:

$V_{OUT} = V_{IN} + V_L$

We can then establish the relationship:

$V_{OUT} = V_{IN} \times (1 + t_{ON}/t_{OFF})$

using the relationship for duty cycle (D):

$t_{ON}/(t_{ON} + t_{OFF}) = D$

Then for the boost circuit:

$$\mathbf{V_{OUT} = V_{IN}/(1-D)}$$

Similar derivations can be had for the buck circuit:

$$\mathbf{V_{OUT} = V_{IN} \times D}$$

and for the inverter circuit (flyback):

$$\mathbf{V_{OUT} = V_{IN} \times D/(1-D)}$$

Control Techniques

From the derivations for the boost, buck, and inverter (flyback), it can be seen that changing the duty cycle controls the steady-state output with respect to the input voltage. This is a key concept governing all inductor-based switching circuits.

The most common control method, shown in **Figure 7**, is pulse-width modulation (PWM). This method takes a sample of the output voltage and subtracts this from a reference voltage to establish a small error signal (V_{ERROR}). This error signal is compared to an oscillator ramp signal. The comparator outputs a digital output (PWM) that operates the power switch. When the circuit output voltage changes, V_{ERROR} also changes and thus causes the comparator threshold to change. Consequently, the output pulse width (PWM) also changes. This duty cycle change then moves the output voltage to reduce to error signal to zero, thus completing the control loop.

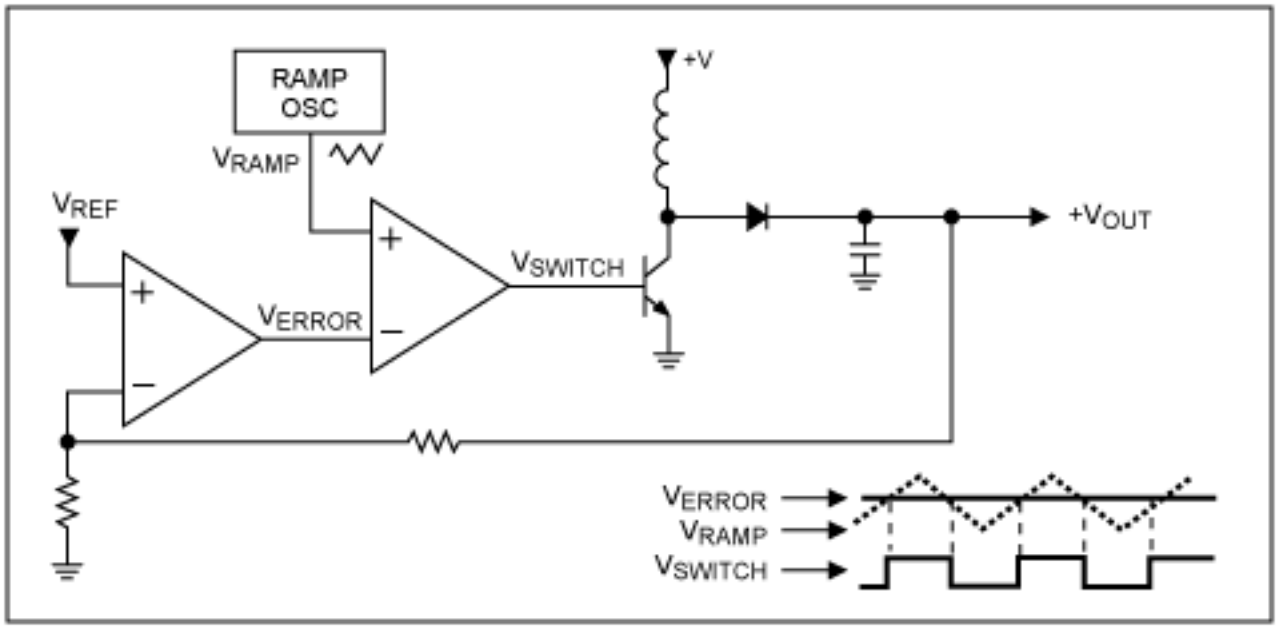

Figure 7. Varying error signal generates a pulse-width-modulated switch signal.

Figure 8 shows a practical circuit using the boost topology formed with the MAX1932. This IC is an integrated controller with an onboard programmable digital-to-analog converter (DAC). The DAC sets the output voltage digitally through a serial link. R5 and R8 form a divider that meters the output voltage. R6 is effectively out of circuit when the DAC voltage is the same as the reference voltage (1.25V). This is because there is zero volts across R6 and so zero current. When the DAC output is zero (ground), R6 is effectively in parallel with R8. These two conditions correspond to the minimum and maximum output adjustment range of 40V and 90V, respectively.

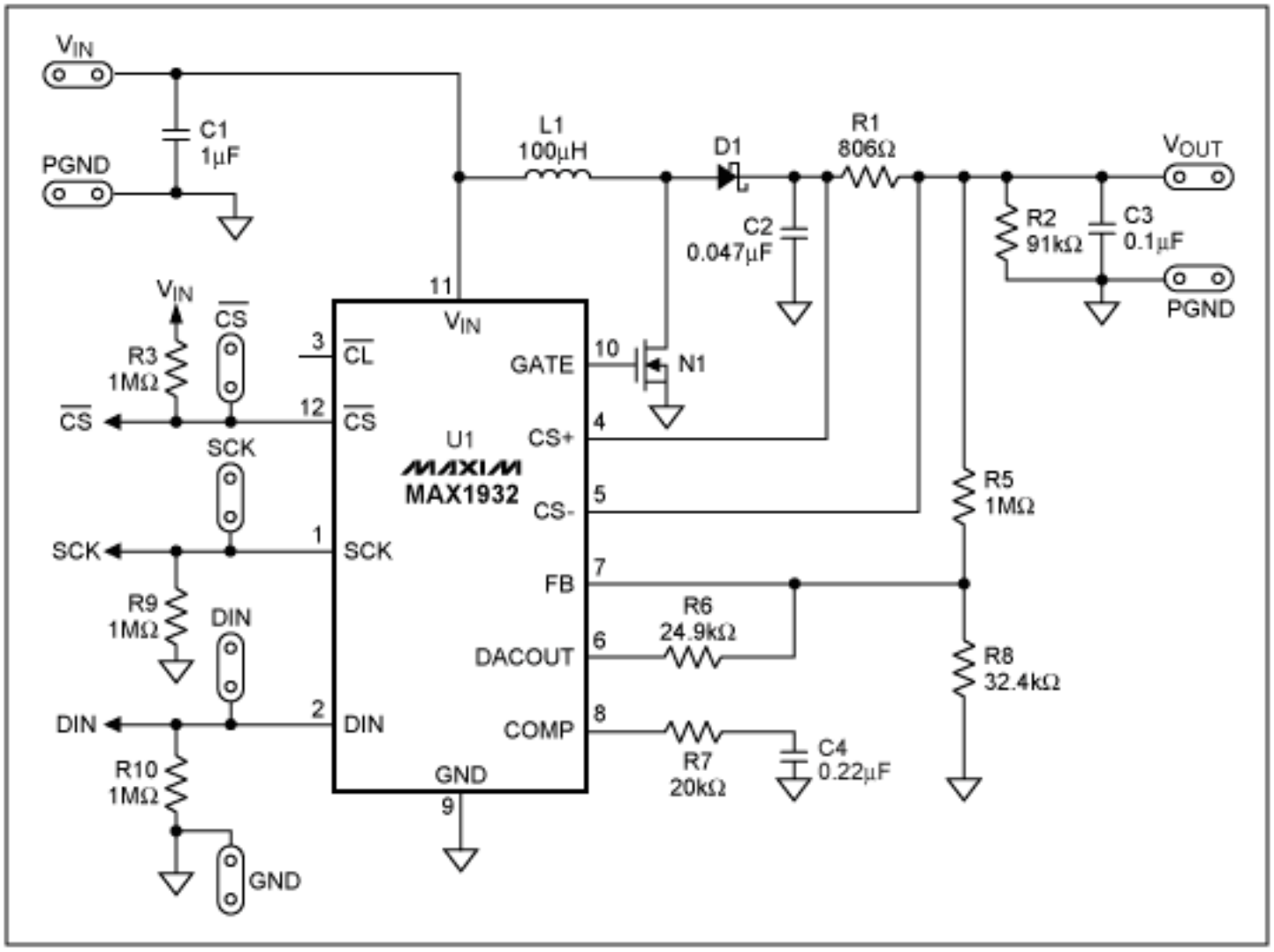

Figure 8. The MAX1932 provides an integrated boost circuit with voltage-mode control.

Next, the divider signal is subtracted from the internal 1.25V reference and then amplified. This error signal is then output on pin 8 as a current source. This, in conjunction with the differential input pair, forms a transconductance amplifier. This arrangement is used because the output at the error amp is high impedance (current source), allowing the circuit's gain to be adjusted by changing R7 and C4. This arrangement also provides the ability to trim the loop gain for acceptable stability margins. The error signal on pin 8 is then forwarded to the comparator and output to drive the power switch. R1 is a current-sense resistor that meters the output current. When the current is unacceptably high, the PWM circuit shuts down, thereby protecting the circuit.

The type of switching (topology) in Figures 7 and 8 is classified as a voltage-mode controller (VMC) because the feedback regulates the output voltage. For analysis we can assume that if the loop gain is infinite, the output impedance for an ideal voltage source is zero. Another commonly used type of control is current-mode control (CMC). This method regulates the output current and, with infinite loop gain, the output is a high-impedance source. In CMC, the current loop is nested with a slower voltage loop, as shown in **Figure 9**; a ramp is generated by the slope of the inductor current and compared with the error signal. So, when the output voltage sags, the CMC supplies more current to the load. The advantage of CMC is its ability to manage the inductor current. In VMC the inductor current is not metered. This becomes a problem because the inductor, in conjunction with the output filter capacitor, forms a resonant tank that can ring and even cause oscillations. Current mode control senses the inductor current to correct for inconsistencies. Although difficult to accomplish, carefully selected compensation components can effectively cancel out this resonance in VCM.

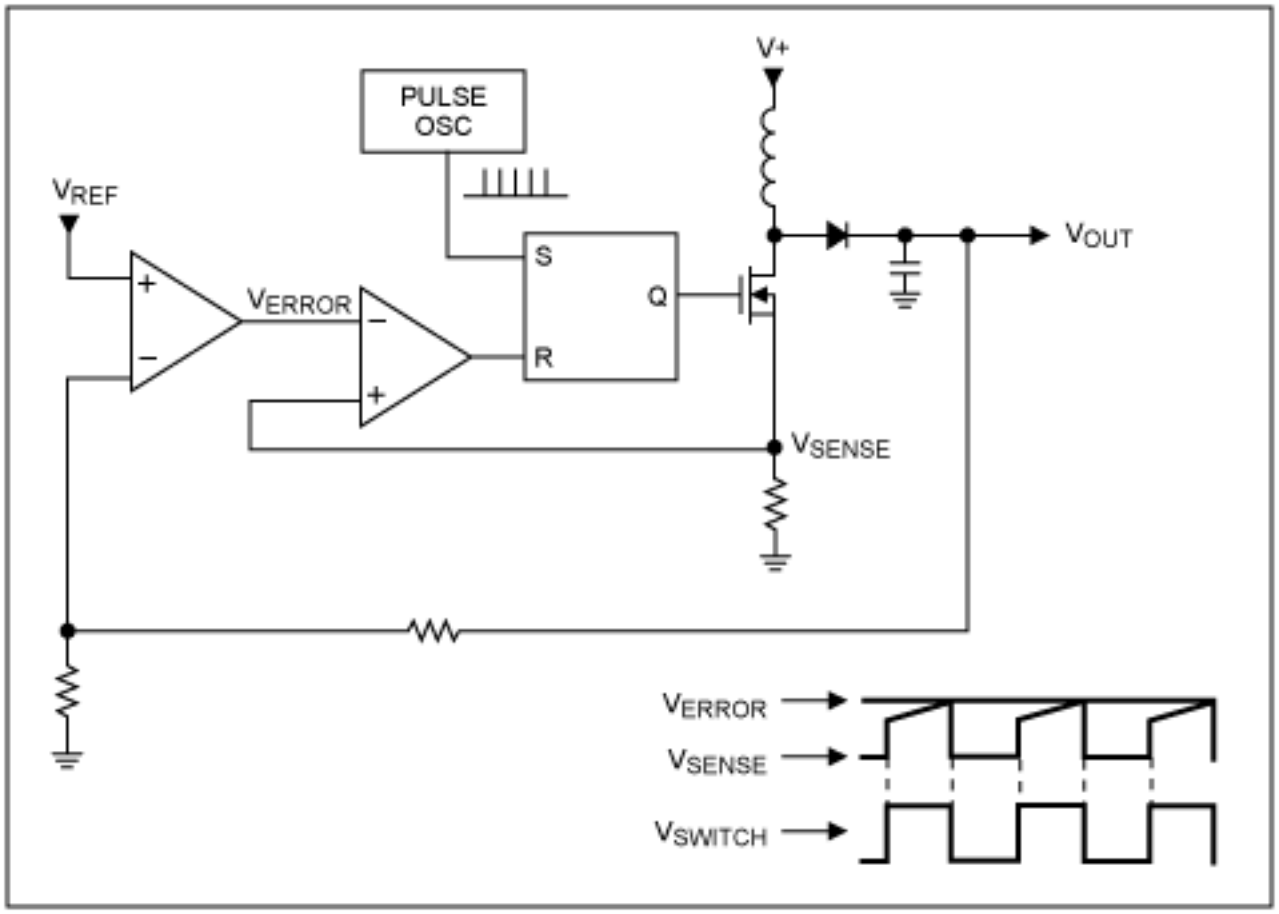

Figure 9. Current-mode pulse-width modulation.

The circuit in **Figure 10** uses CMC with the MAX668 controller. This boost circuit is similar to Figures 7 and 8 except that R1 senses the inductor current for CMC. R1 and some internal comparators provide a current limit. R5 in conjunction with C9 filters the switching noise on the sense resistor to prevent false triggering of the current limit. The MAX668's internal current-limit threshold is fixed; changing the resistor, R1, adjusts the current-limit setting. The resistor, R2, sets the operating frequency. The MAX668 is a versatile integrated circuit that can provide a wide range of DC-DC conversions.

The external components of the MAX668 can have high-voltage ratings that provide greater flexibility for high-power applications. For portable applications that require less power, the MAX1760 and MAX8627 are recommended. These latter devices use internal FETs, and sense the current by using the FETs' resistance to measure inductor current (no sense resistor required).

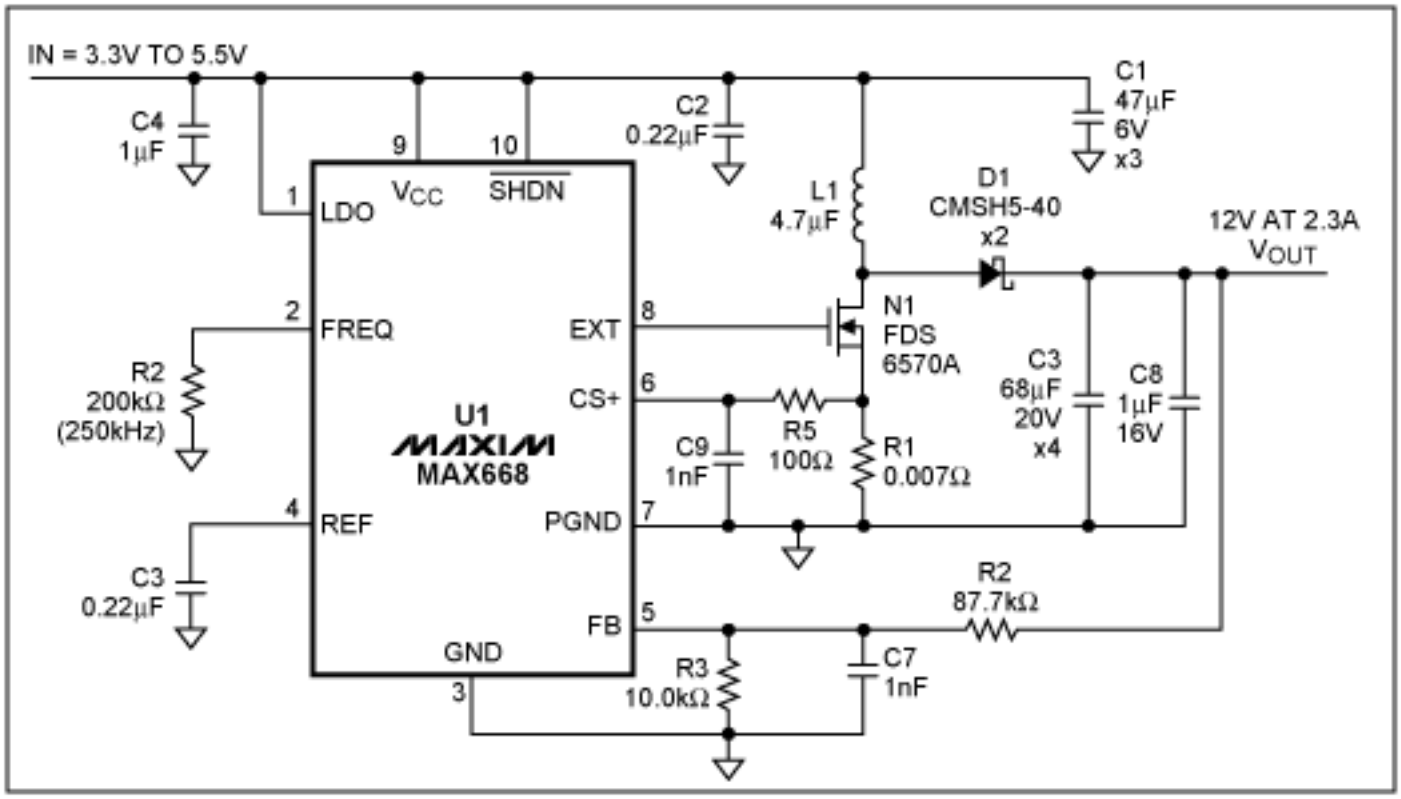

Figure 10.MAX668 for current-mode-controlled boost circuit.

Figure 11 shows a simplified version of Maxim's Quick-PWM™ architecture. To analyze this buck circuit, we start with the feedback signal below the regulating threshold defined by the reference. If there are no forward current faults, then the t_{ON} one-shot timer that calculates the on-time for DH is turned on immediately along with DH. This t_{ON} calculation is based on the output voltage divided by the input, which approximates the on-time required to maintain a fixed switching frequency defined by the constant K. Once the t_{ON} one-shot timer has expired, DH is turned off and DL is turned on. Then if the voltage is still below the regulating threshold, the DH immediately turns back on. This allows the inductor current to rapidly ramp up to meet the load requirements. Once equilibrium with the load has been met, the average inductor voltage must be zero. Therefore we calculate:

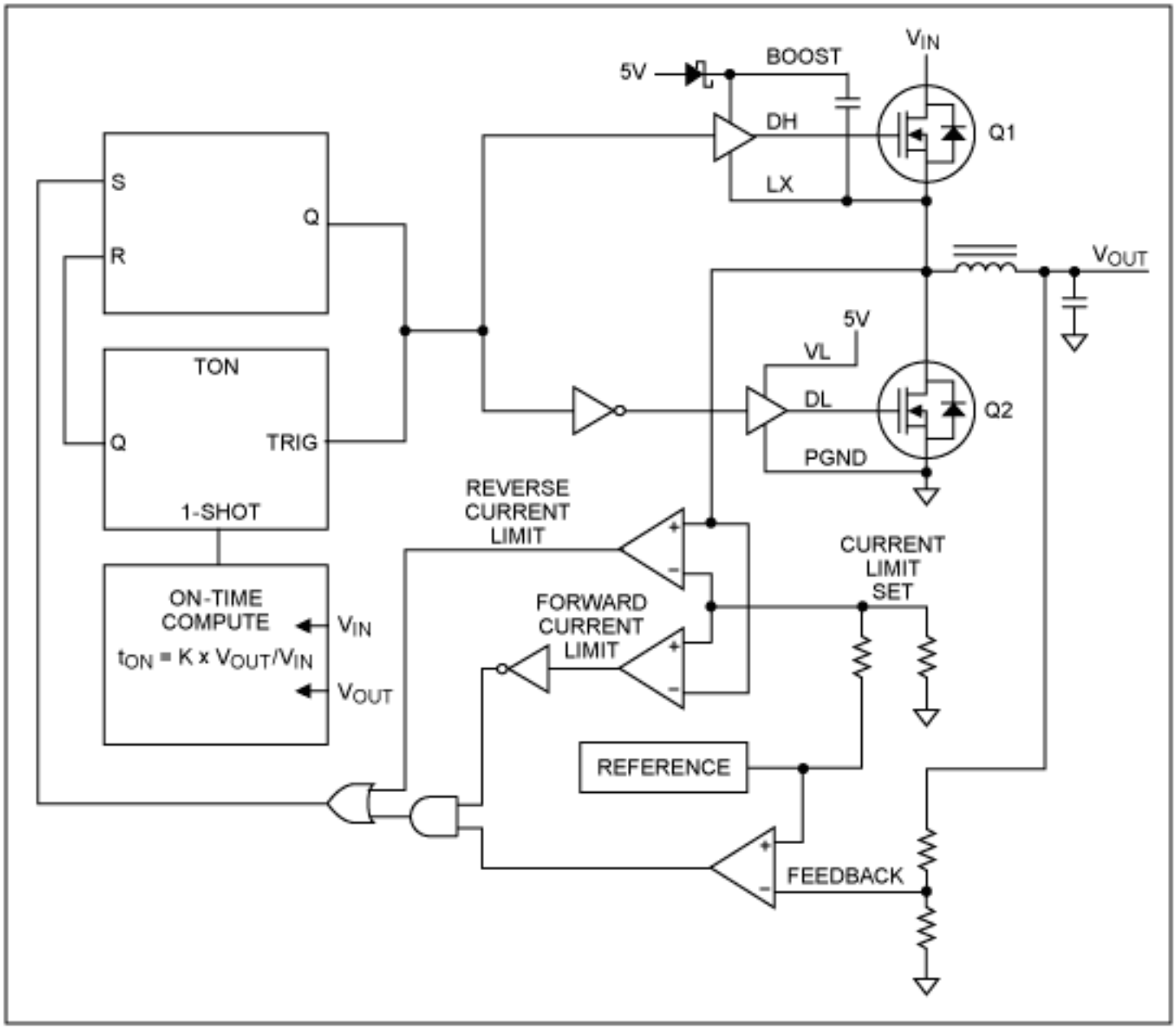

Figure 11. Simplified block diagram of Maxim's Quick-PWM control.

$t_{ON} \times (V_{IN} - V_{OUT}) = t_{OFF} \times V_{OUT}$

Rearranging:

$V_{OUT}/(V_{IN}-V_{OUT}) = t_{ON}/t_{OFF}$

Adding 1 to both side and collecting terms:

$V_{OUT}/V_{IN} = t_{ON}/(t_{ON} + t_{OFF})$

Because the duty factor is D:

$t_{ON}/(t_{ON} + t_{OFF}) = D$

For the buck circuit:

$D = V_{OUT}/V_{IN}$

Maxim's proprietary Quick-PWM control method offers some advantages over PWM. Quick-PWM control

generates a new cycle when the output voltage falls below the regulation threshold. Consequently, heavy transients force the output to fall, immediately firing a new on-cycle. This action results in a 100ns load-step response. It is also important to note that unlike the buck circuit in Figure 1, Figure 11 uses a MOSFET (Q2) instead of a diode for the discharge path. This design reduces the losses associated with the diode drop; the on-resistance of the MOSFET channel doubles as a current sense. Because output-voltage ripple is required to stimulate the circuit to switch, an output filter capacitor with some ESR is required to maintain stability. The Quick-PWM architecture can also respond quickly to line input changes by directly feeding the input voltage signal to the on-time calculator. Other methods must wait for the output voltage to sag or soar before action is taken, and this is often too late.

A practical application of Quick-PWM is found in **Figure 12**. The MAX8632 is an integrated DDR memory power supply. Along with a Quick-PWM buck circuit (VDDQ), the MAX8632 integrates a high-speed linear regulator (VTT) to manage bus transients found in DDR memory systems. The linear regulator offers specific advantages over switchers: linear regulators do not have an inductor to limit current slew-rate, so a very fast current slew rate can service load transients. Slower circuits would require large capacitors to provide load current until the power supply can ramp up the current to service the load.

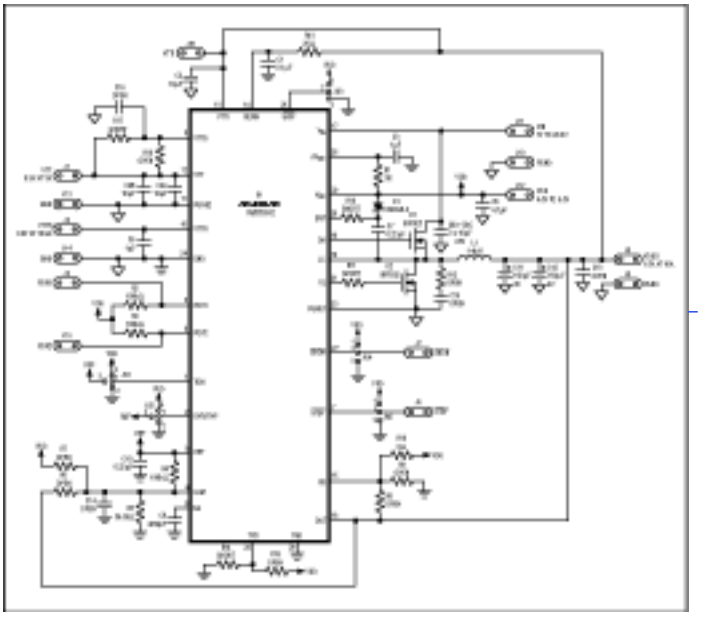

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Figure 12. The MAX8632 uses Maxim's Quick-PWM architecture and a linear regulator to provide a complete DDR power-supply system. The device can be used as a main GPU, or standard core-logic power supply.

Efficiency

One of the largest power-loss factors for switchers is the rectifying diode. The power dissipated is simply the forward voltage drop multiplied by the current going through it. The reverse recovery for silicon diodes can also create loss. These power losses reduce overall efficiency and require thermal management in the form of a heat sink or fan.

To minimize this loss, switching regulators can use Schottky diodes that have a relatively low forward-voltage drop and good reverse recovery. For maximum efficiency, however, you can use a MOSFET switch instead of the diode. This design is known as a 'synchronous rectifier' (see **Figures** 11, 12 and **13**). The synchronous rectifier switch is open when the main switch is closed, and the same is true conversely. To prevent cross-conduction (both top and bottom switches are on simultaneously), the switching scheme must be break-before-make. Because of this, a diode is still required to conduct during the interval between the opening of the main switch and the closing of the synchronous-rectifier switch (dead time). When a MOSFET is used as a synchronous switch, the current normally flows in reverse (source to drain), and this allows the integrated body diode to conduct current during the dead time. When the synchronous rectifier switch closes, the current flows through the MOSFET channel. Because of the very low-channel resistance for power MOSFETs, the standard forward drop of the rectifying diode can be reduced to a few millivolts. Synchronous rectification can provide efficiencies well above 90%

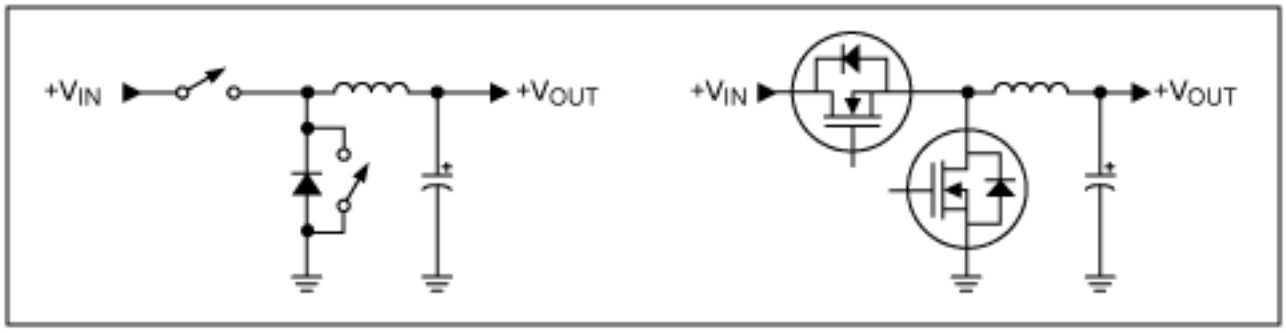

Figure 13. Synchronous rectification for the buck circuit. Notice the integrated MOSFET body diode.

Skip Mode Improves Light Load Efficiency

A feature offered in many modern switching controllers is skip mode. Skip mode allows the regulator to skip cycles when they are not needed, which greatly improves efficiency at light loads. For the standard buck circuit (Figure 1) with a rectifying diode, not initiating a new cycle simply allows the inductor current or inductor energy to discharge to zero. At this point the diode blocks any reverse-inductor current flow and the voltage across the inductor goes to zero. This is called "discontinuous mode" and is shown in **Figure 14**. In skip mode, a new cycle is initiated when the output voltage drops below the regulating threshold. While in skip mode and discontinuous operation, the switching frequency is proportional to the load current. The situation with a synchronous rectifier is, unfortunately, somewhat more complicated. This is because the inductor current can reverse in the MOSFET switch if the gate is left on. The MAX8632 integrates a comparator that senses when the current through the inductor has reversed and opens the switch, allowing the MOSFET's body diode to block the reverse current.

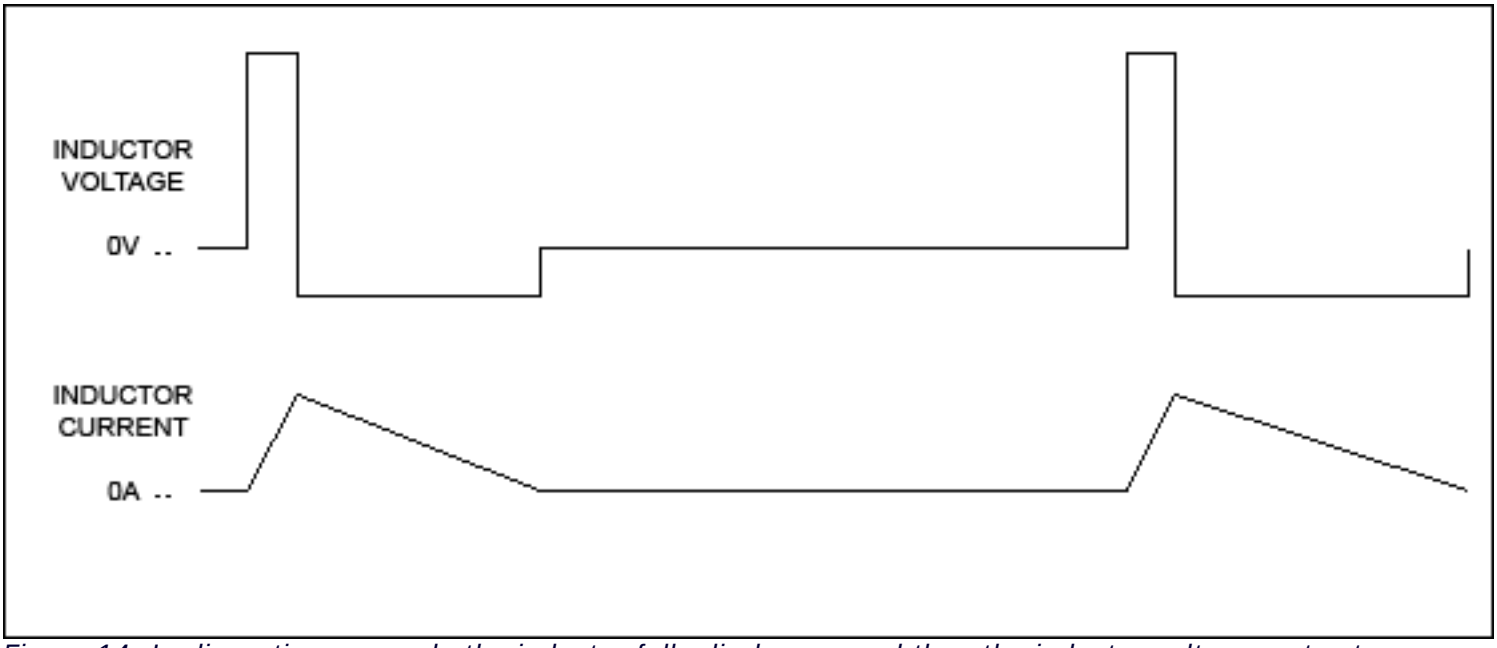

Figure 14. In discontinuous mode the inductor fully discharges and then the inductor voltage rests at zero.

Figure 15 shows that skip mode offers improved light-load efficiencies but at the expense of noise, because the switching frequency is not fixed. The forced-PWM control technique maintains a constant switching frequency, and varies the ratio of charge cycle to discharge cycle as the operating parameters vary. Because the switching frequency is fixed, the noise spectrum is relatively narrow, thereby allowing simple lowpass or notch filter techniques to greatly reduce the peak-to-peak ripple voltage. Because the noise can be placed in a less-sensitive frequency band, PWM is popular with telecom and other applications where noise interference is a concern.

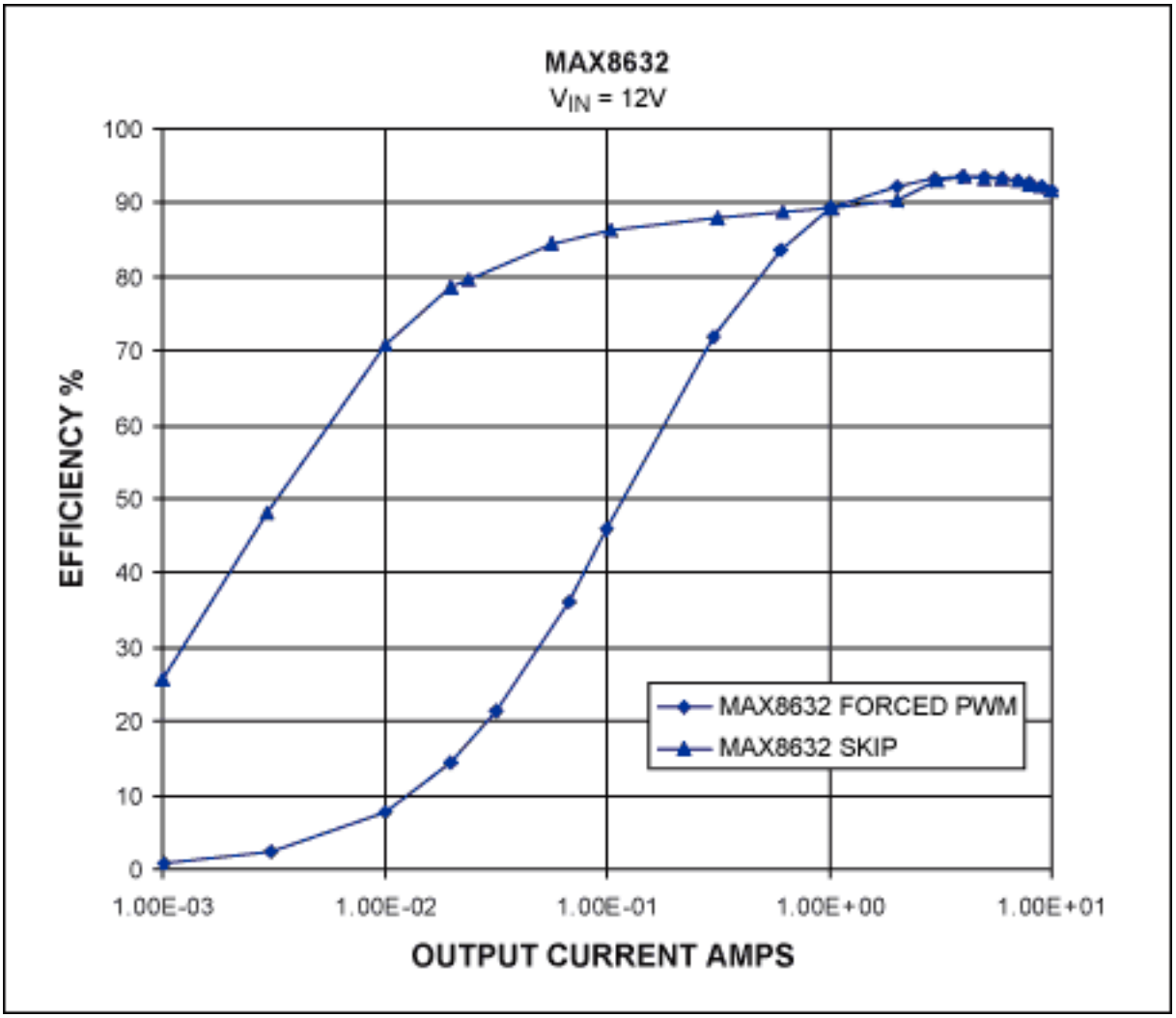

Figure 15. Efficiency with and without skip mode.

Summary

Although switching techniques are more difficult to implement, switching circuits have almost completely replaced linear power supplies in a wide range of portable and stationary designs. This is because switching circuits offer better efficiency, smaller components, and fewer thermal management issues.

MOSFET power switches are now integrated with controllers to form single-chip solutions, like the MAX1945 circuit shown in **Figure 16**. This chip has a metallic slug on the underside that removes heat from the die so the 28-pin TSSOP package can dissipate over 1W, allowing the circuit to supply over 10W to its load. With a 1MHz switching frequency, the output inductor and filter capacitors can be reduced in size, further saving valuable space and component count. As MOSFET power-switch technologies continue to improve, so will switch-mode performance, further reducing cost, size, and thermal management problems.

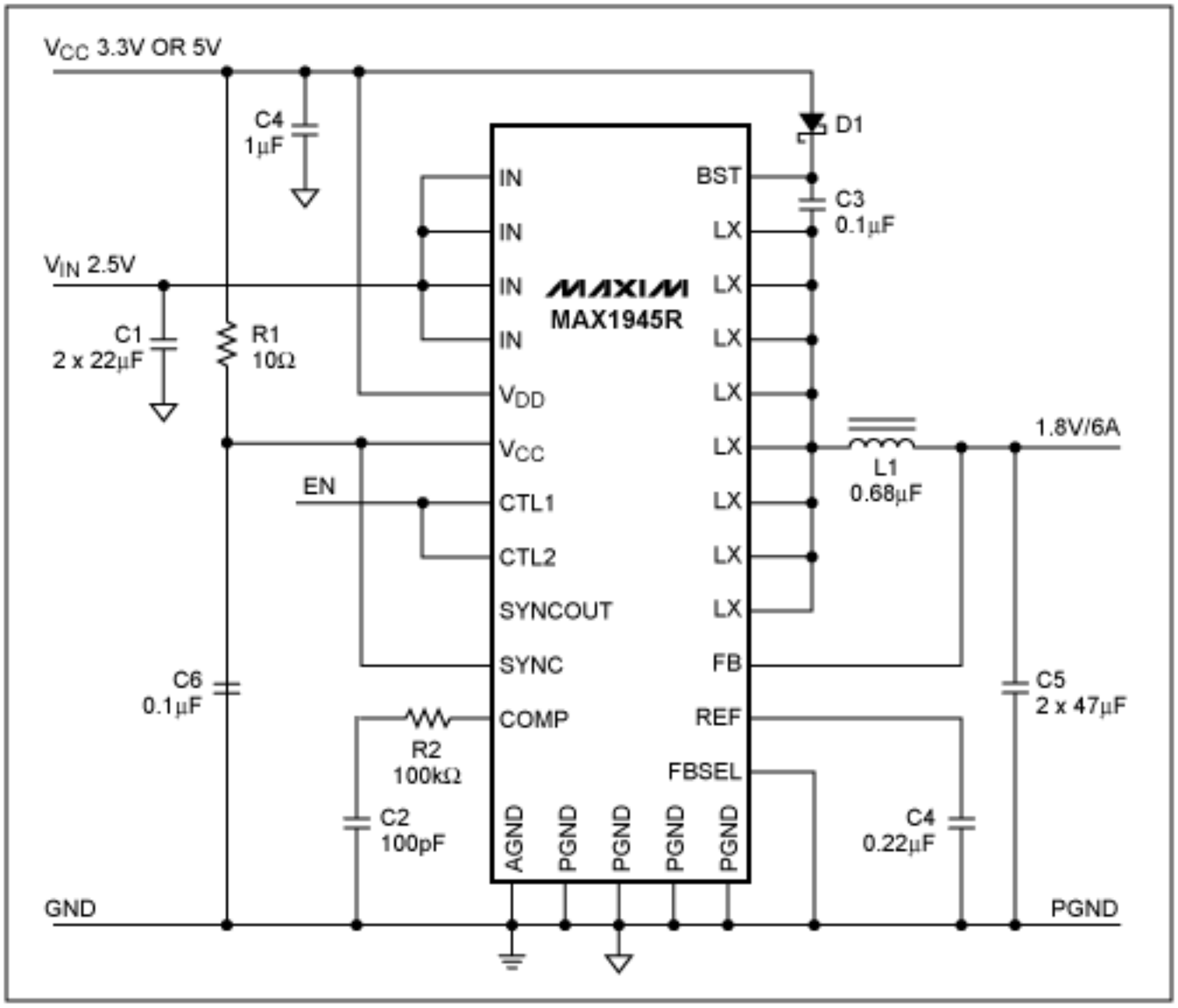

Figure 16. The MAX1945 is a 6A internal switch device with a reduced part count and small footprint to save board space.

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Related Parts

MAX1932: QuickView -- Full (PDF) Data Sheet -- Free Samples

MAX668: QuickView -- Full (PDF) Data Sheet -- Free Samples

MAX8632: QuickView -- Full (PDF) Data Sheet -- Free Samples

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DC-DC Switching Converters: Modeling and Control

Ali Altowati

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  - *Averaging Small-Signal Modeling*
  - *Closed-loop Analysis*
- *QFT Controller Synthesis*
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  - *Closed-Loop Performance Specifications*
  - *QFT Loop-shaping controller*
- *Performance Validation and Simulation*
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Introduction

- *Switched-mode power converters* (SMPC) are used efficiently to convert power between different voltage and current levels.
- A switching converter is a circuit that uses a power switch, an inductor, and a diode to transfer energy from input to output.
- Buck and boost are basic topologies of switched-mode power converters.
- Switching-mode converters are widely used today to provide power processing for applications ranging from computing and communications to medical electronics, appliance control, transportation, and high-power transmission.
- They offer higher efficiency than traditional linear power supplies.
- Modeling and simulation generally form an integral part of any power converter design process, which should significantly improve performance and reduce costs.

Introduction

- Switching regulators have to provide robust behavior in spite of load variations or input voltage perturbations and must exhibit a perfect tracking of the reference voltage.
- Numerous control strategies for designing robust controllers for switching converters have been proposed to find a successful and practical feedback control method and they are mainly based on optimal control theory.
- But such techniques usually need tedious work to find appropriate weighting functions, and they often result in high order controllers.
- Among the robust control techniques that are being currently investigated in power electronics is the quantitative feedback theory (QFT) approach.
- Developed by Isaac Horowitz in 1960s.
- Frequency domain technique utilizing the Nichols chart (NC) in order to achieve a desired robust design over a specified region of plant uncertainty .

Introduction

- The design process is very transparent allowing a designer to see what trade-offs are necessary to achieve the desired performance.
- The QFT method has already been applied in the design of different types of control systems, e.g., flight control and robot control systems.

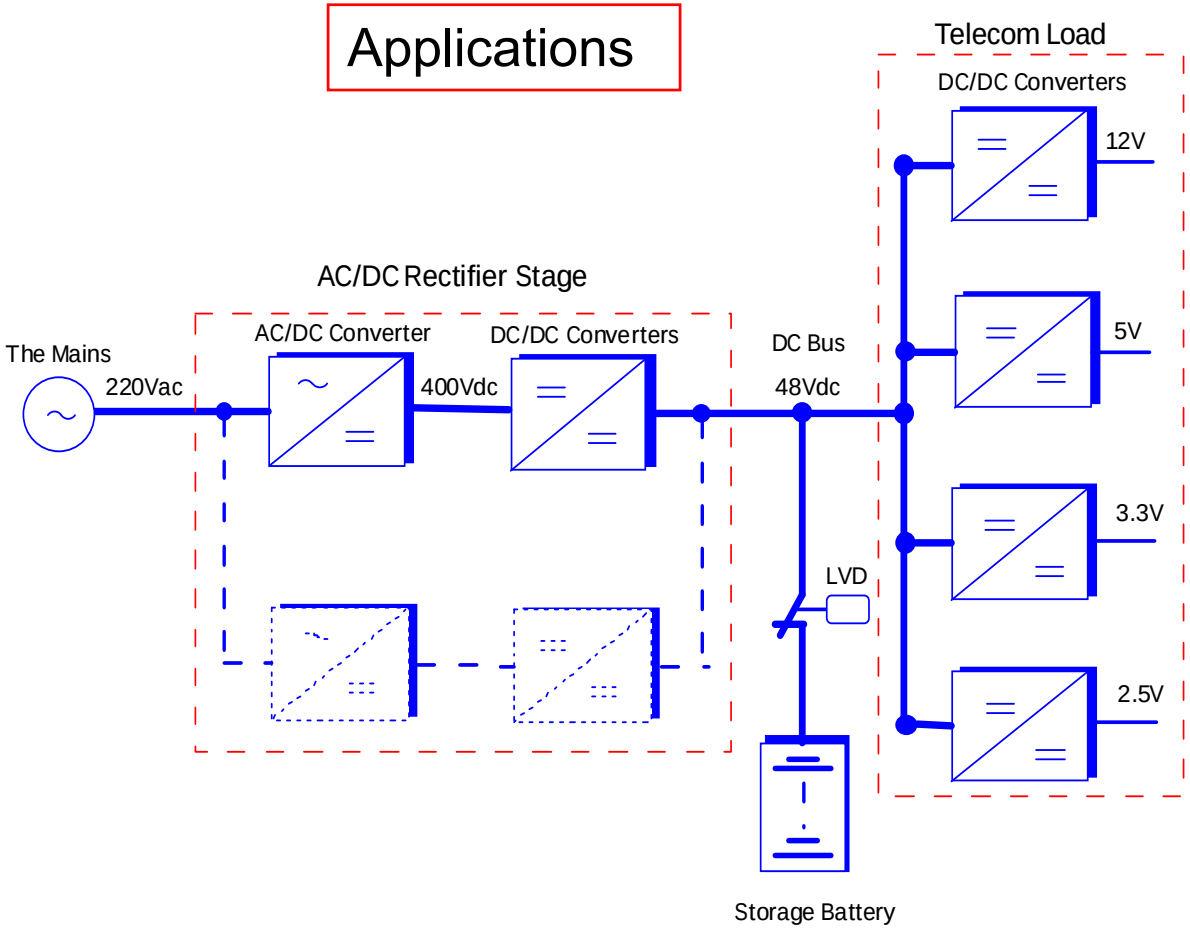
- In this work, the QFT approach is adopted to design a robust controller for switching-mode buck converter, that

✓ Maximizing the bandwidth of the control loop,

✓ Minimizing the effects of load disturbances over the specified region of plant uncertainties and load disturbances.

Introduction

Applications

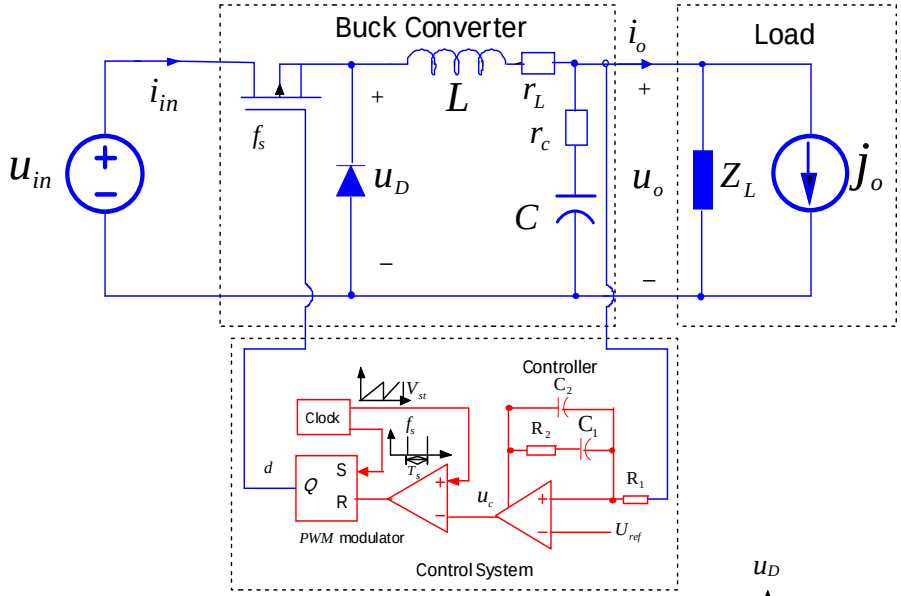


A typical telecom power systems

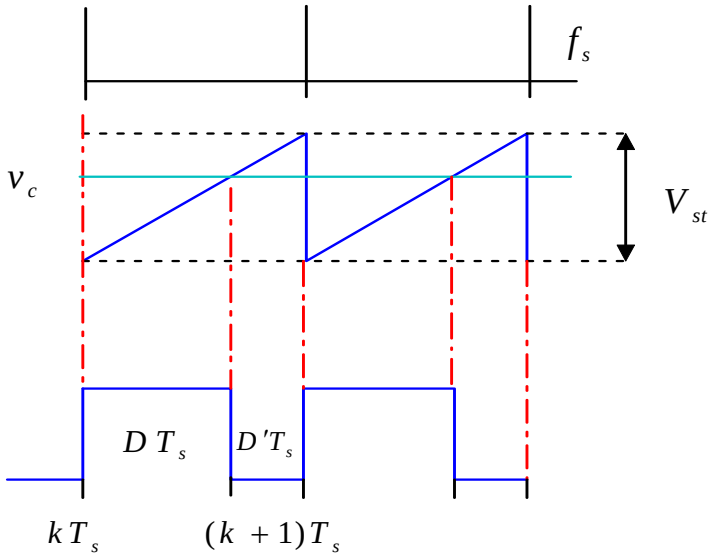
Introduction

- The buck converter is one of the simplest and mostly used among power converters: a chopper circuit that converts a dc input to a lower dc output voltage

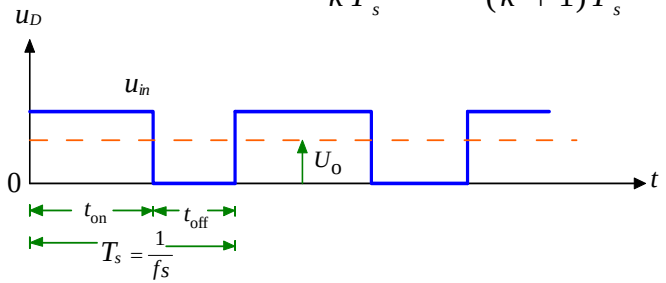
Buck converter circuit



Duty-ratio generation



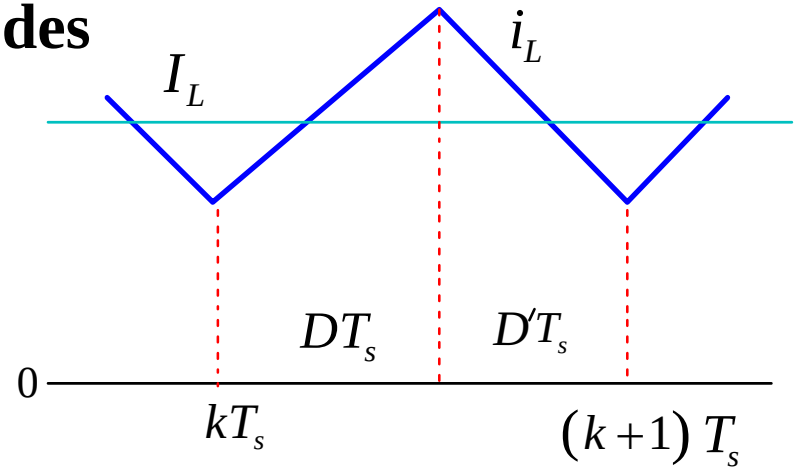
$$D = t_{on} / T_s$$



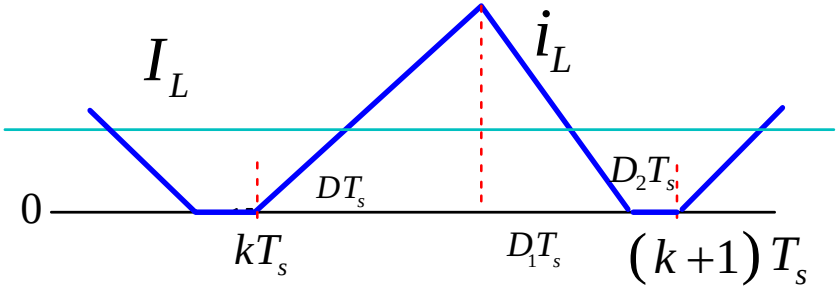
Introduction

- **Classification of operation modes**

1. Continuous conduction mode CCM



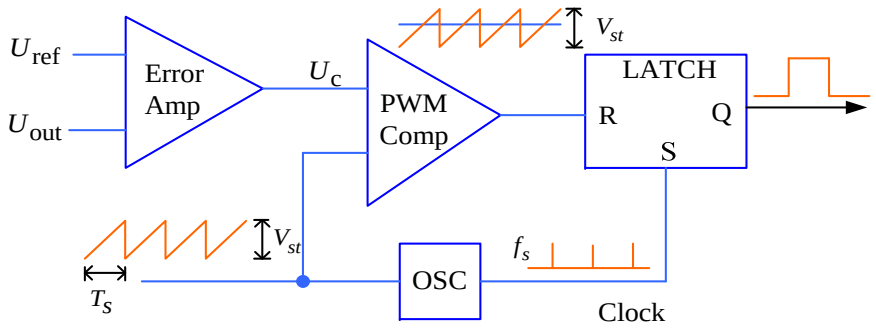
2. Discontinuous conduction mode DCM



Introduction

- **Control Structures of DC/DC Converter**

1. Voltage mode control VMC

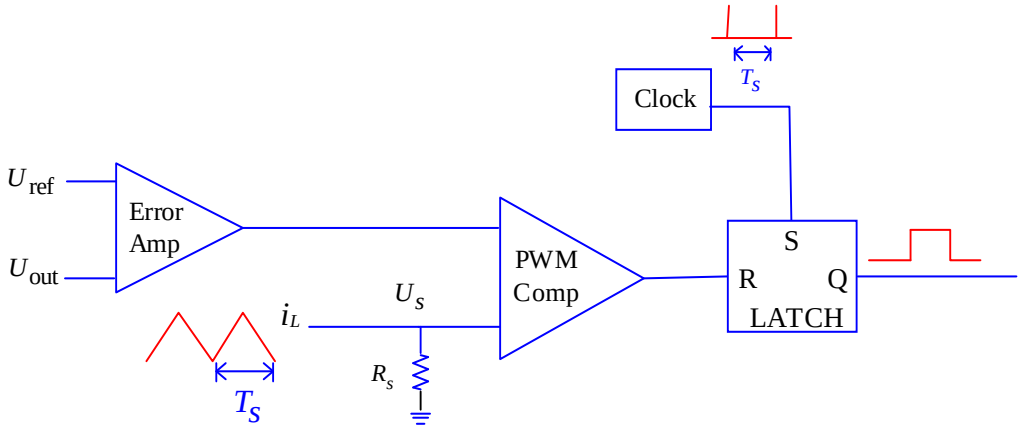


(+) A single feedback loop is easier to design and analyze.
(-) Any change in line or load must first be sensed as an output change and then corrected by the feedback loop. This means usually slow a response.

Introduction

- **Control Structures of DC/DC Converter**

2. Current mode control CMC



(+) Since inductor current rises with a slope determined by u_{in} - u_o, this waveform will respond immediately to line voltage changes, eliminating both the delayed response and gain variation with changes in input voltage.
(-) The control loop becomes unstable at duty cycles above 50% unless slope compensation is added.

Modeling of dc-dc switching power converters

- The inherent switching operation of power converters results in the circuit components being connected together in periodically changing configurations.
- Each configuration being described by a separate set of equations.
- The transient analysis and control design for converters is therefore difficult since a number of equations must be solved in sequence.
- The averaging technique provides a solution to this problem.

Small-signal averaging technique:

- It is the most common averaging technique.
- It gives clear physical insight which is helpful in the analysis and design of converters.
- In state-space averaging (SSA), the switching circuit is divided into two (CCM) or three (DCM) different structures.
- The derivatives of inductor currents and capacitor voltages are defined based on circuit theory for every substructure.
- These currents and voltages are averaged over one switching cycle.

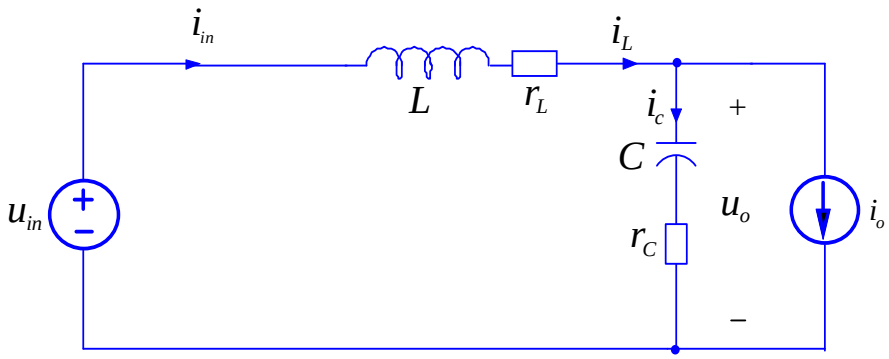
On-time

$$\frac{d_{iL}}{dt} = -\frac{r_C + r_L}{L} \cdot i_L - \frac{1}{L} \cdot u_C + \frac{1}{L} \cdot u_{in} + \frac{r_C}{L} \cdot i_o$$

$$\frac{du_C}{dt} = \frac{1}{C} \cdot i_L - \frac{1}{C} \cdot i_o$$

$$u_o = r_C \cdot i_L + u_C - r_C \cdot i_o$$

$$i_{in} = i_L$$



On-time subcircuit

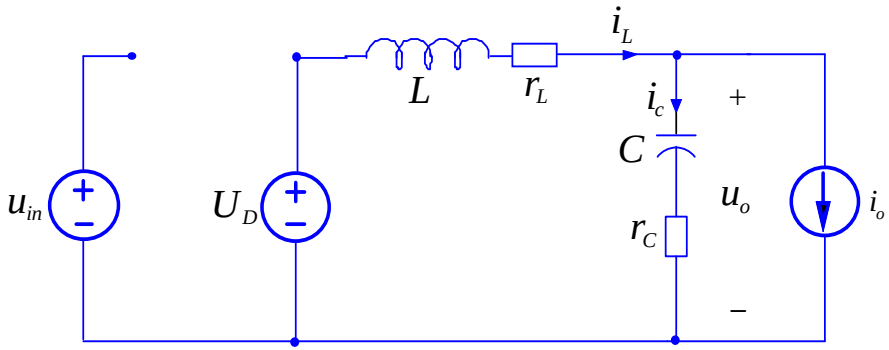
Off-time

$$\frac{di_L}{dt} = -\frac{r_C + r_L}{L} \cdot i_L - \frac{1}{L} \cdot u_C - \frac{1}{L} \cdot U_D + \frac{r_C}{L} \cdot i_o$$

$$\frac{du_C}{dt} = \frac{1}{C} \cdot i_L - \frac{1}{C} \cdot i_o$$

$$u_o = r_C \cdot i_L + u_C - r_C \cdot i_o$$

$$i_{in} = 0$$



Off-time subcircuit

State-space averaging

- The averaged state-space equations are obtained by multiplying the on-time and off-time equations by *d* and *d´=1-d* respectively:

$$\frac{d_{iL}}{dt} = -\frac{r_C + r_L}{L} \cdot i_L - \frac{1}{L} \cdot u_C + \frac{d}{L} \cdot u_{in} - \frac{d'}{L} \cdot U_D + \frac{r_C}{L} \cdot i_o$$

$$\frac{du_C}{dt} = \frac{1}{C} \cdot i_L - \frac{1}{C} \cdot i_o$$

$$u_o = r_C \cdot i_L + u_C - r_C \cdot i_o$$

$$i_{in} = d.i_L$$

Linearization

- Averaged models are nonlinear and need to be linearized by using conventional linearizing methods.

$$\frac{d_{iL}}{dt} = -\frac{(r_L + r_C)}{L}\cdot\hat{i}_L - \frac{1}{L}\cdot\hat{u}_C + \frac{D}{L}\cdot\hat{u}_{in} + \frac{r_C}{L}\cdot\hat{i}_o + \frac{U_o + U_D}{L}\cdot\hat{d}$$

$$\frac{d\hat{u}_C}{dt} = \frac{1}{C}\cdot\hat{i}_L - \frac{1}{C}\cdot\hat{i}_o$$

$$u_o = r_C\cdot i_L + \hat{u}_C - r_C\cdot i_o$$

$$i_{in} = D.\hat{i}_L + I_L\cdot\hat{d}$$

$$\dot{\hat{\mathbf{x}}} = \mathbf{A}\hat{\mathbf{x}} + \mathbf{B}\hat{\mathbf{u}}$$

$$\hat{\mathbf{y}} = \mathbf{C}\hat{\mathbf{x}} + \mathbf{D}\hat{\mathbf{u}}$$

$$\hat{\mathbf{x}} = \begin{bmatrix}\hat{i}_L & \hat{u}_C\end{bmatrix},\ \hat{\mathbf{u}} = \begin{bmatrix}\hat{i}_{in} & \hat{i}_o & \hat{d}\end{bmatrix},\ \hat{\mathbf{y}} = \begin{bmatrix}\hat{i}_{in} & \hat{u}_o\end{bmatrix}^T$$

Unterminated transfer functions

- The open-loop transfer function model of the buck converter can be obtained by inserting the modulator equation into the power stage . According to the matrix algebra, we can solve the system as follows

$$\mathbf{X}(s) = (sI - \mathbf{A})^{-1}\mathbf{B}\cdot\mathbf{U}(s)$$

Input dynamics

$$\mathbf{Y}(s) = \left(\mathbf{C}\left(sI - \mathbf{A}\right)^{-1}\mathbf{B} + \mathbf{D}\right)\cdot\mathbf{U}(s)$$

Output dynamics

Open-loop

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{u}_o \end{bmatrix} = \begin{bmatrix} Y^*_{in-o} & T^*_{ji-o} & G^*_{ci} \\ G^*_{io-o} & -Z^*_{o-o} & G^*_{co} \end{bmatrix} \begin{bmatrix} \hat{u}_{in} \\ \hat{i}_o \\ \hat{c} \end{bmatrix}$$

Definitions

$$Y^*_{in-o} = \left.\frac{\hat{i}_{in}}{\hat{u}_{in}}\right|_{\hat{i}_o,\hat{c}=0}$$ input admittance,

$$T^*_{ji-o} = \left.\frac{\hat{i}_{in}}{\hat{i}_o}\right|_{\hat{u}_{in},\hat{c}=0}$$ Output-to-input transfer function

$$G^*_{ci} = \left.\frac{\hat{i}_{in}}{\hat{c}}\right|_{\hat{u}_{in},\hat{i}_o=0}$$ Control-to-input transfer function,

$$G^*_{io-o} = \left.\frac{\hat{u}_o}{\hat{u}_{in}}\right|_{\hat{i}_o,\hat{c}=0}$$ Line-to-output transfer function

$$Z^*_{o-o} = \left.\frac{\hat{u}_o}{\hat{i}_o}\right|_{\hat{u}_{in},\hat{c}=0}$$ Output impedance,

$$G^*_{co} = \left.\frac{\hat{u}_o}{\hat{c}}\right|_{\hat{u}_{in},\hat{i}_o=0}$$ Control-to-output transfer function

control signal : $\hat{c} = \hat{u}_c$

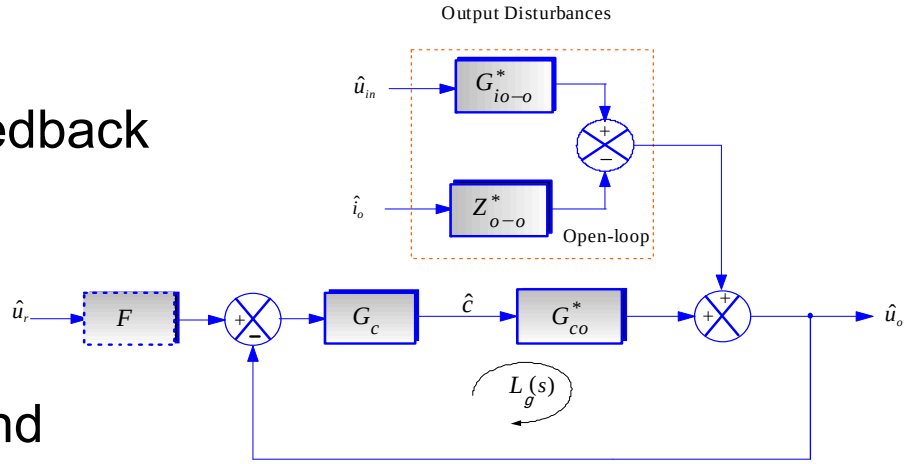
VMC : $\hat{d} = \frac{1}{V_{st}}\hat{u}_c$

Steady-state operating point

$$I_L = I_o$$
$$I_{in} = DI_L$$
$$U_o = DU_{in} - U_D D' - r_L I_L$$
$$U_C = U_o$$

❑ Closed-loop analysis

- Two degree-of-freedom (TDOF) feedback voltage-mode control structure



- The closed-loop responses due to changes in the reference voltage $\hat{u}_r$, and disturbance input voltage $\hat{u}_{in}$, and output current $\hat{i}_o$ are given by

$$T = \frac{\hat{u}_o}{\hat{u}_r} = \frac{FL_g}{1+L_g}, \quad T_{D1} = \frac{\hat{u}_o}{\hat{u}_{in}} = \frac{G^*_{io-o}}{1+L_g}, \quad \text{and} \quad T_{D2} = \frac{\hat{u}_o}{\hat{i}_o} = -\frac{Z^*_{o-o}}{1+L_g}$$

- The output-voltage-loop gain is $L_g(s)$

$$L_g(s) = G_c G^*_{co}$$

QFT Controller Synthesis

- In order to apply the proposed method, it is necessary to specify the required tolerances on the acceptable closed-loop responses **T**, $\mathbf{T_{D1}}$ and $\mathbf{T_{D2}}$ in the frequency domain. The performance specifications of interest here are:

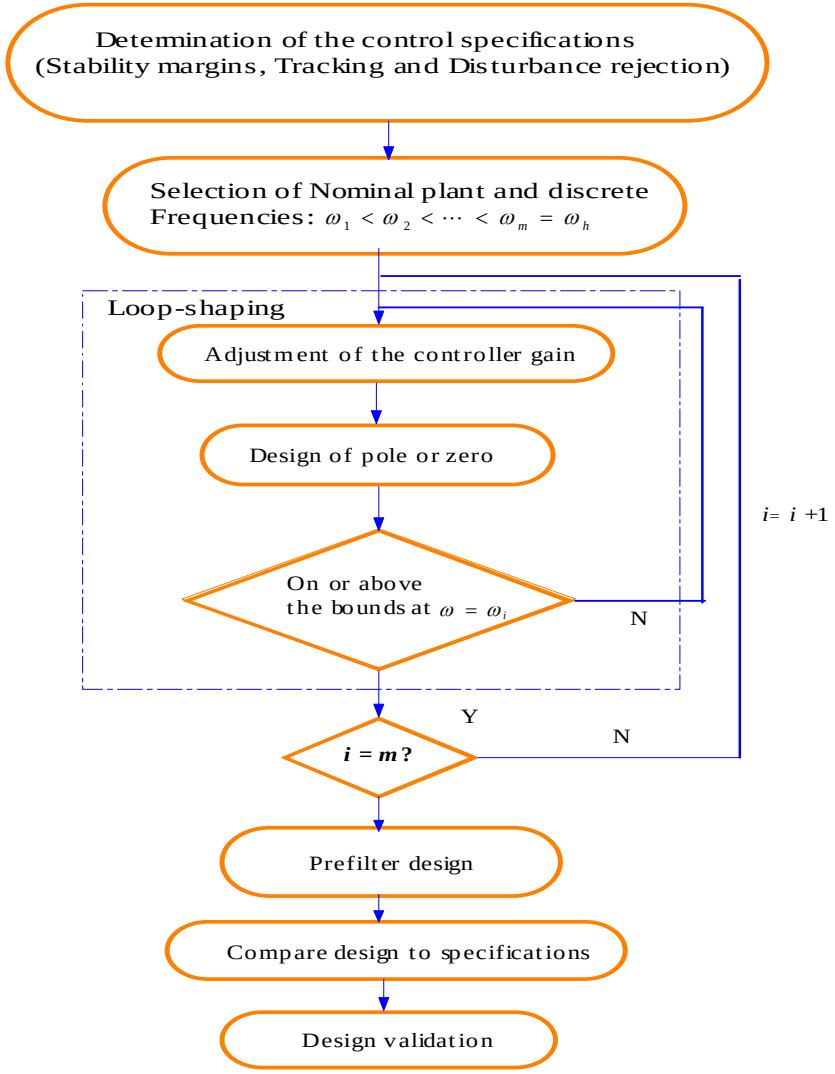
  (1) *Robust Stability*, (2) *Reference Tracking*, (3) *Disturbance Rejection.*

- These specifications are used to compute the frequency dependent QFT bounds, $B(\omega)$, that guide the shaping of the nominal loop transmission

$$L_{g_{nom}} = G_c G_{co_{nom}}$$

QFT Controller Synthesis

Flowchart of the proposed QFT control design



QFT Controller Synthesis

❑ Template generation

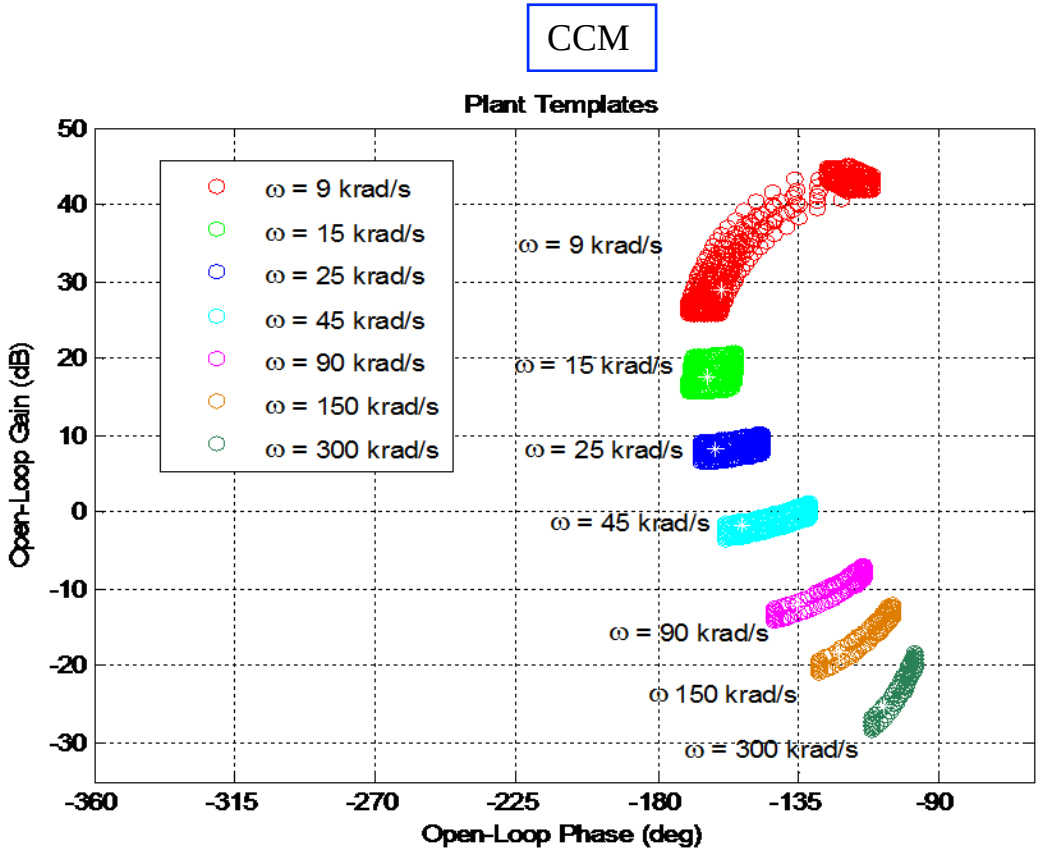
- If the system is not defined by a single model, but rather has several due to the parametric uncertainty,
- The frequency responses of the system for a given frequency are represented by a set of points, as many as there are different models. All of these points define a region of uncertainty known as template.
- The plant templates are plotted on the Nichols chart at the useful desired frequency

Nominal model parameters of buck converter and their ranges

Uncertain parameter	U_o	U_{in}	P_{out}	L	C	r_C	r_L	U_D	r_{ds}	r_d
Nominal value	10V	50V	30W	105μH	316μF	33mΩ	0.06mΩ	0.3V	400mΩ	55mΩ
Variations	Λ	20-70V	10%:90%	±50%	±20%	+90%	+90%	±20%	+90%	+90%

QFT Controller Synthesis

- Template generation



QFT Controller Synthesis

Closed-Loop Performance Specifications

(1) Robust Stability: To ensure robust stability of the closed-loop system, the following constraint on the peak magnitude of the closed loop frequency responses is set:

$$\left|\frac{\mathbf{L_g}}{1+\mathbf{L_g}}\right| \le \gamma, \qquad \forall G_{co}^{*} \in \mathbf{G_{co}^{*}}$$

Specification $\gamma = 1.2$ gives minimum gain and phase margins of 5.26 dB and 49° respectively.

(2) Reference Tracking: An acceptable range of variations in the closed loop tracking responses of the system due to uncertainty and disturbances is defined.

$$\left|T_L(j\omega)\right| \le \left|\mathbf{T}(j\omega)\right| \le \left|T_U(j\omega)\right|, \qquad \forall G_{co}^{*} \in \mathbf{G_{co}^{*}}$$

QFT Controller Synthesis

Closed-Loop Performance Specifications

- $T_L(s)$ and $T_U(s)$ are the equivalent transfer functions of the lower and upper tracking bounds and they are systematically derived from the desired step response of the system with a settling time of less than 0.1 *ms*, an overshoot of less 2 % and a steady state error of less than 0.1 % in step response.

$$T_U(s) = \frac{3.1\times10^4\left(s+1.5\times10^5\right)}{\left(s^2+10.66\times10^4 s+4.66\times10^9\right)},$$

$$T_L(s) = \frac{4.66\times10^{19}}{\left(s+10.66\times10^4\right)\left(s+6.83\times10^4\right)\left(s+5\times10^4\right)}$$

(3) Disturbance Rejection: the sensitivity function is constrained

$$\left|\frac{1}{1+\mathbf{L_g}(j\omega)}\right| \le \left|1/W_s(j\omega)\right|, \qquad \forall G_{co}^* \in \mathrm{G}_{\mathrm{co}}^*$$

QFT Controller Synthesis

Closed-Loop Performance Specifications

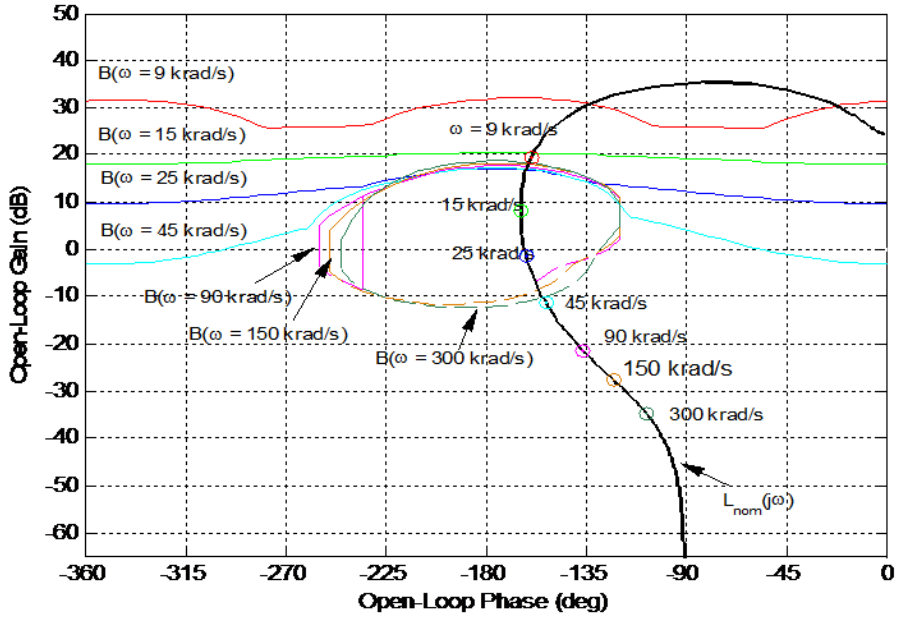
- The design specifications for the performance of the buck converter is a minimum bandwidth frequency of $4.5\text{x}10^4$ rad/s (with a minimum cross-over frequency f_c=10kHz), a maximum steady-state tracking error of 0.035 and a maximum peak magnitude of the sensitivity function of 1.6.

$$W_s(s) = \frac{0.625\left(s^2 + 11.38\times10^3 s + 3.24\times10^9\right)}{\left(s^2 + 1.684\times10^4 s + 7.088\times10^7\right)},$$

QFT Controller Synthesis

❑ Closed-Loop Performance Specifications

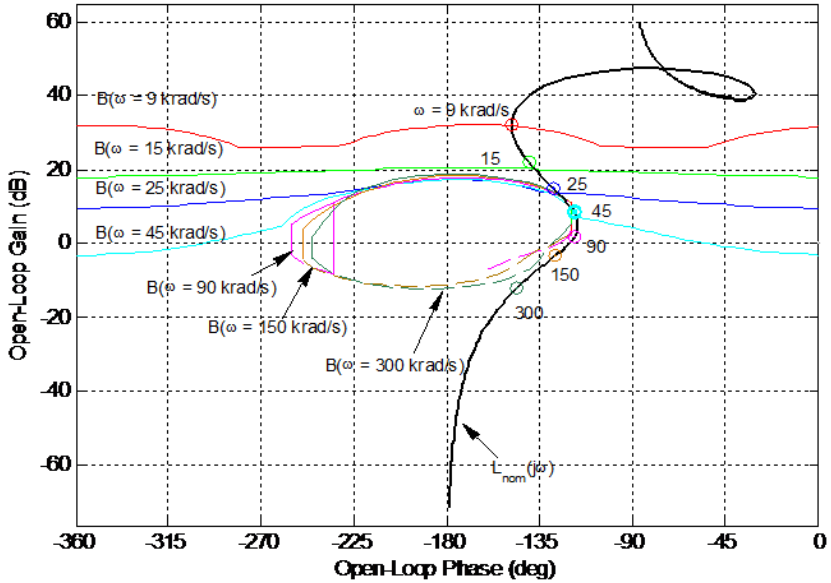
- The intersection of the important QFT bounds B(ω), for each inequality was computed "*The Matlab QFT Frequency Domain Control Design Toolbox"* on the Nichols chart at a number of design frequencies based on plant templates and the performance specifications,



QFT Controller Synthesis

❑ QFT Loop-shaping controller

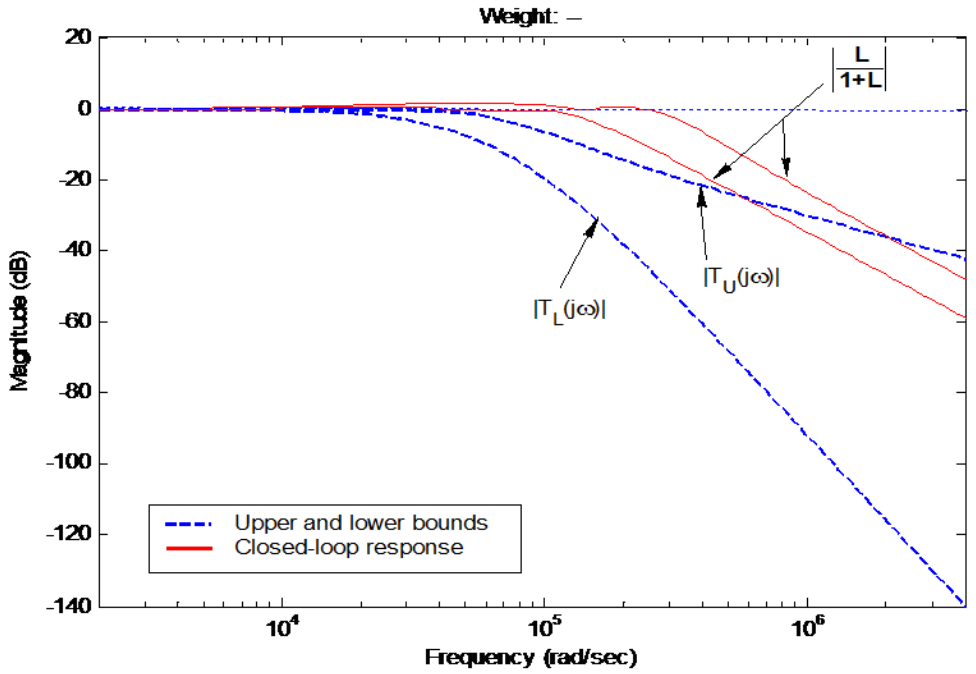
- The objective is to synthesize a controller, G_c, which satisfies the design specifications so that the converter is stable and quickly regulates the output voltage against changes in input voltage or load conditions.
- In general, the controller is designed such that (f_s/10) < f_c < (f_s/5); where f_s is the switching frequency of the converter.



QFT Controller Synthesis

QFT Loop-shaping controller

$$G_c(s) = \frac{5928\left(s/1617+1\right)\left(s/1.7\times10^4+1\right)}{s\left(s/1.766\times10^5+1\right)\left(s/1.369\times10^5+1\right)} = \frac{5928\left(879.5s+14.22\times10^5\right)\left(s+1.7\times10^4\right)}{s\left(s+1.766\times10^5\right)\left(s+1.369\times10^5\right)}$$

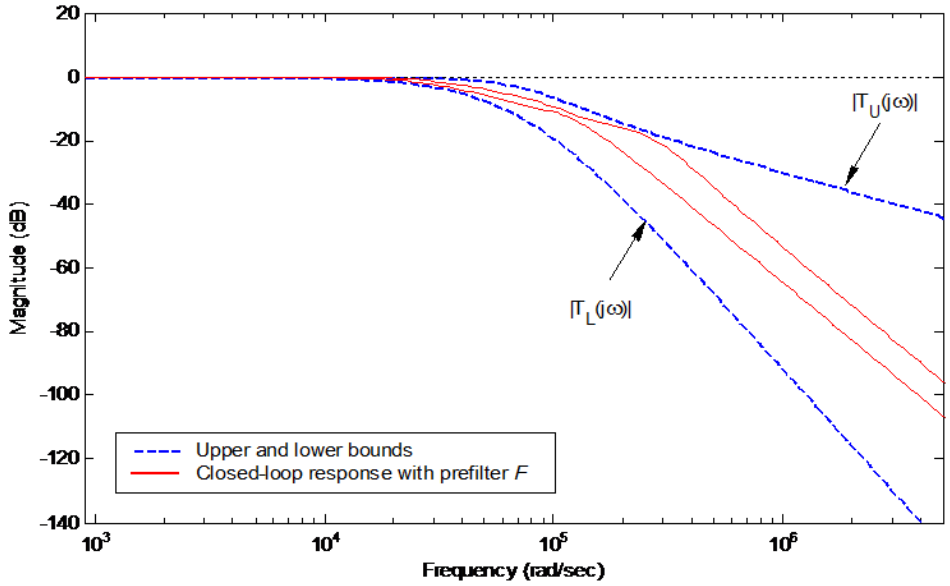


QFT Controller Synthesis

❑ QFT Loop-shaping controller

- Prefilter design *F*: *a dynamic prefilter is required to shape the frequency response to be within the desired range*

$$F(s) = \frac{5.514\times10^4}{s+5.514\times10^4},$$

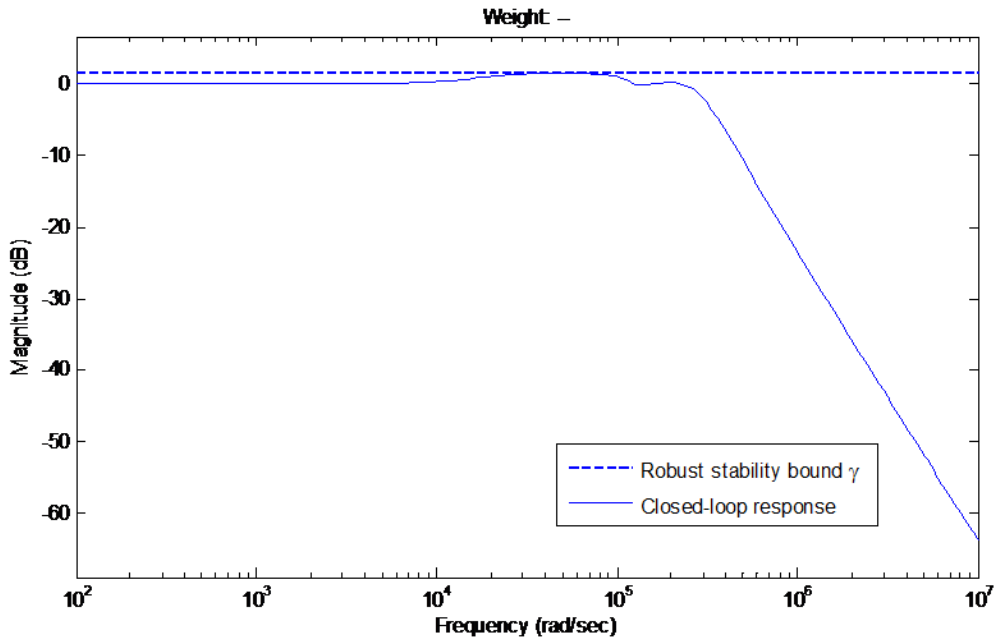


Performance Validation and Simulation

- To verify the design of QFT controller, a validation of the obtained results should be made, graphically checking the specifications in the frequency and time domains.

Frequency-Domain Analysis

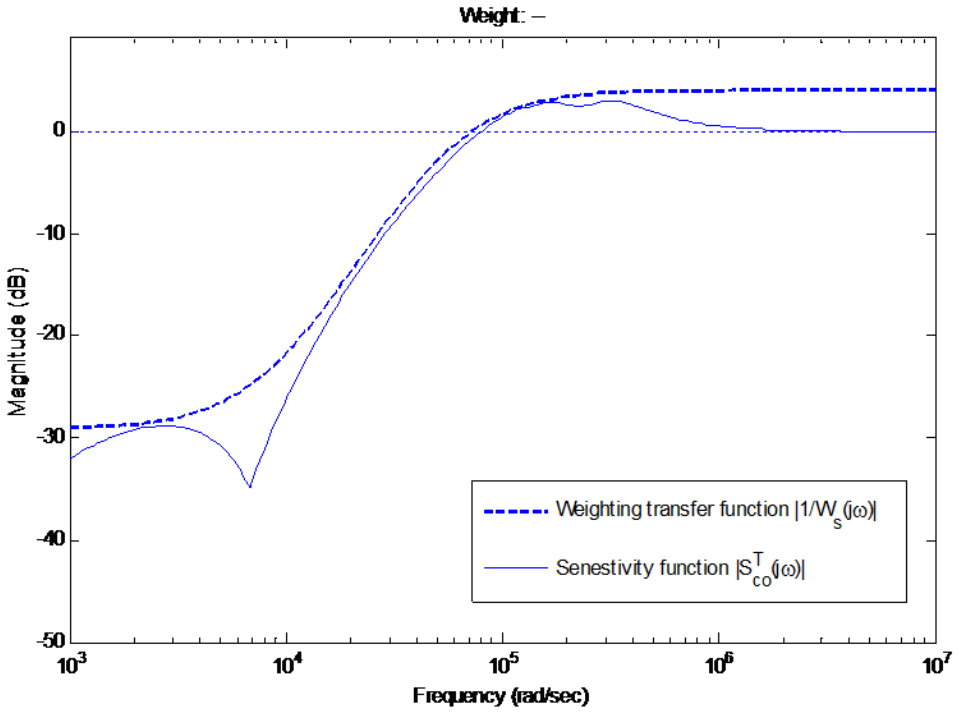
Robust Stability



Performance Validation and Simulation

Disturbance Rejection

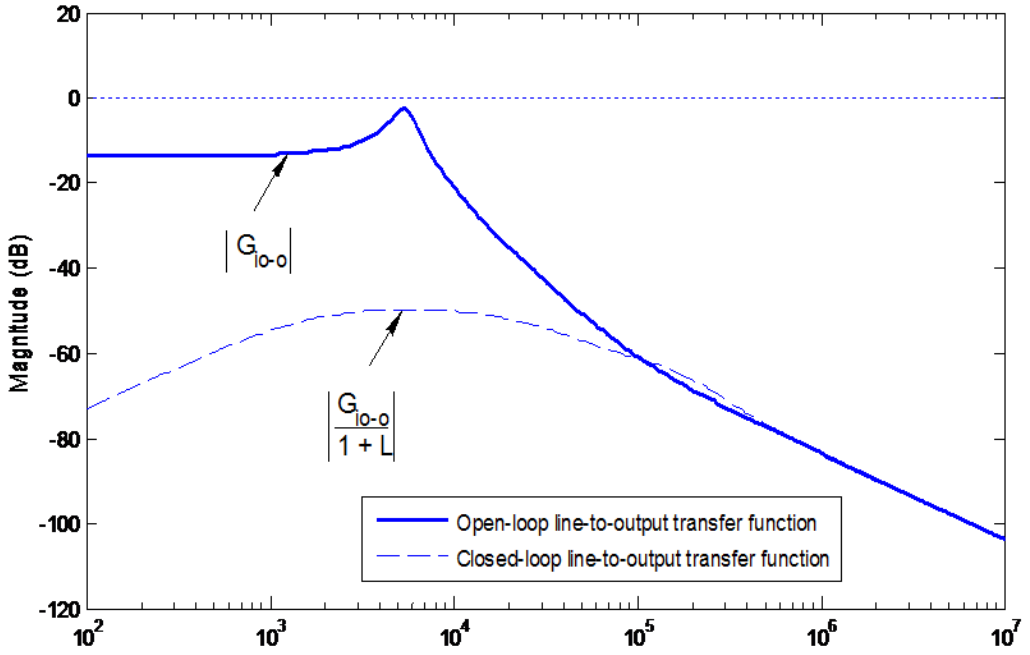
Sensetivity Vs. Weighting transfer function



Performance Validation and Simulation

Disturbance Rejection

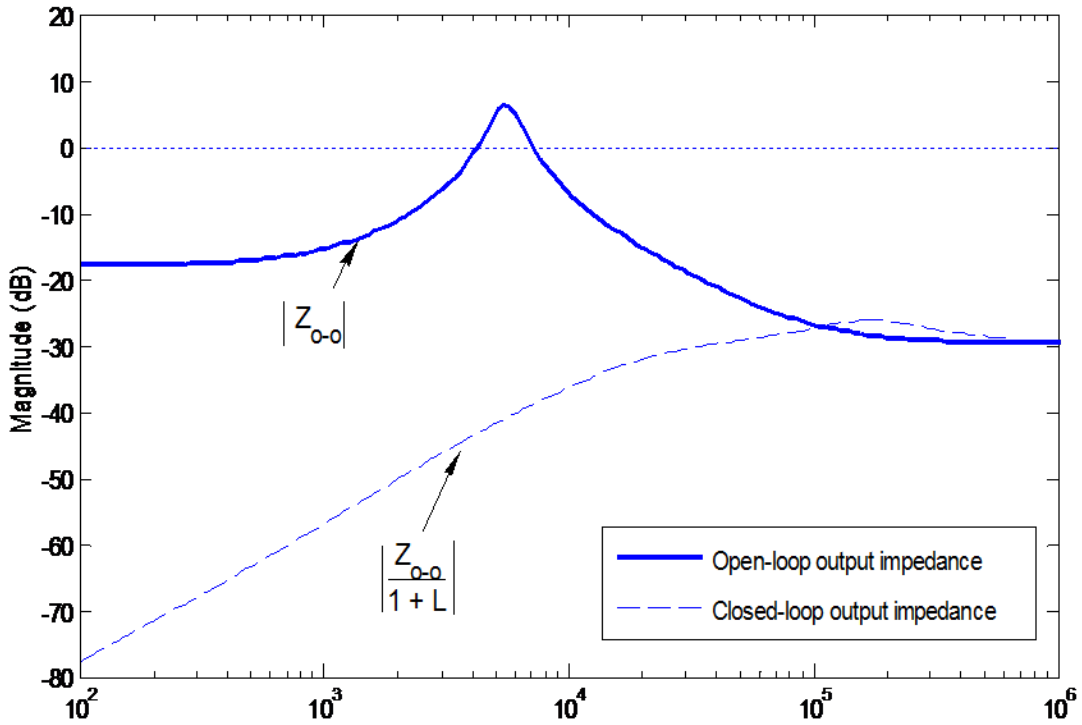
The input-output voltage-disturbance attenuation



Performance Validation and Simulation

Disturbance Rejection

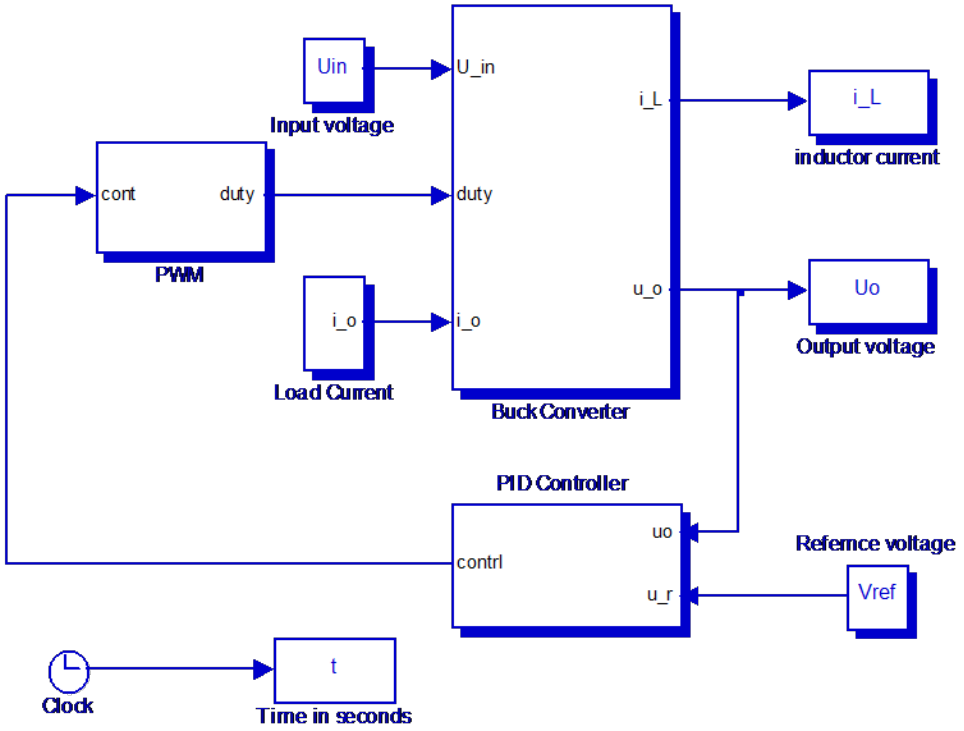
The output impedance



Performance Validation and Simulation

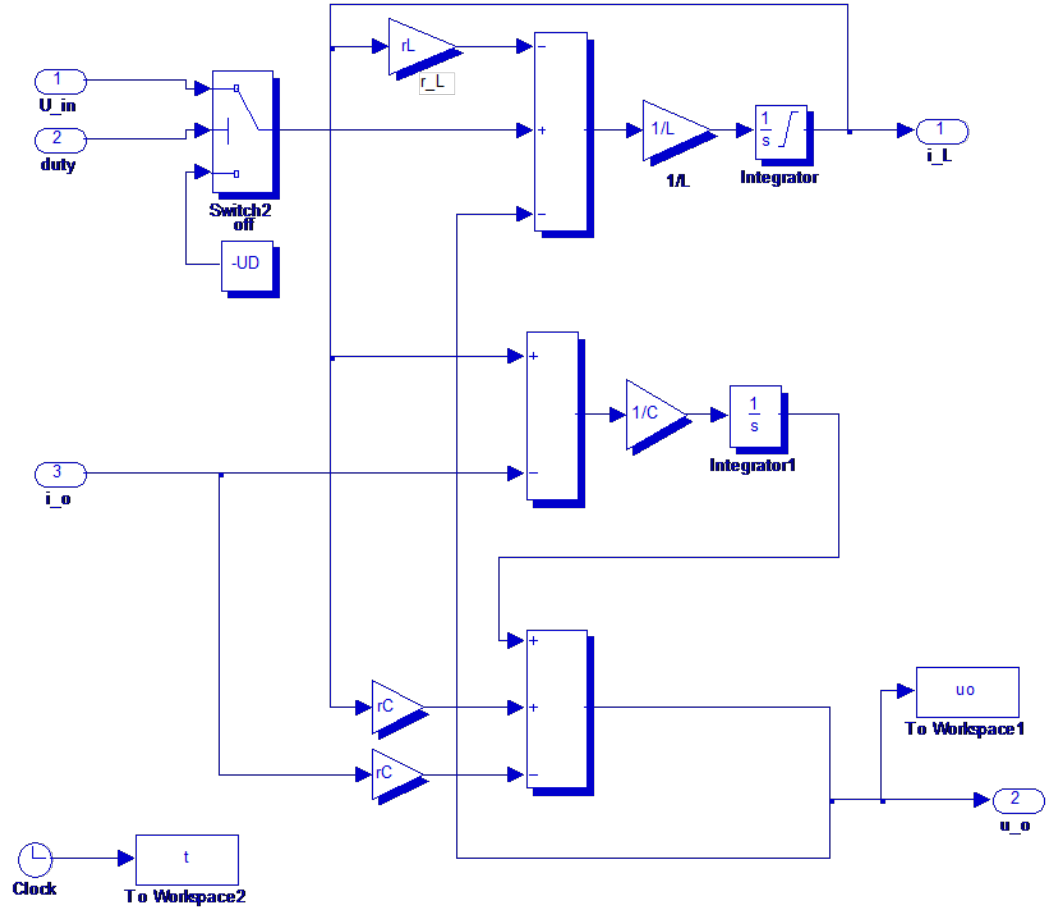
Simulation Tools: Matlab™ Simulink

Voltage mode control VMC



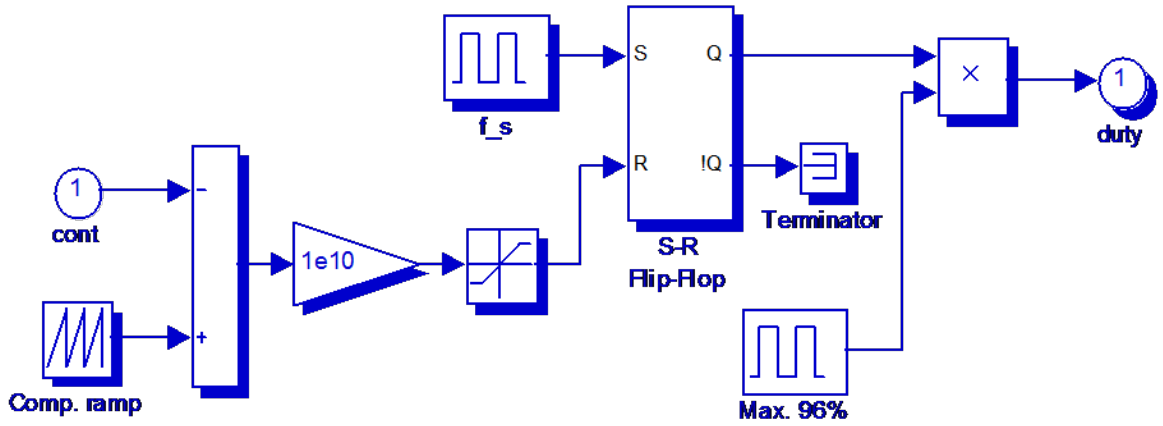
Performance Validation and Simulation

Power Converter averaged model



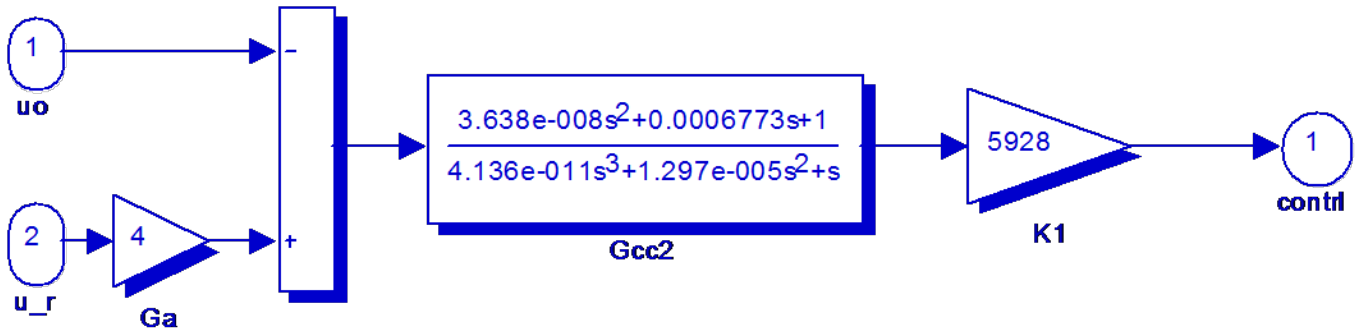
Performance Validation and Simulation

PWM model VMC



Performance Validation and Simulation

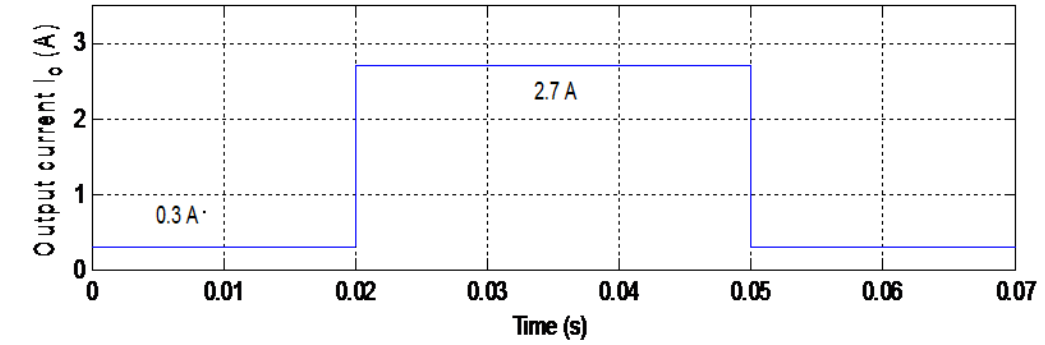
Controller VMC

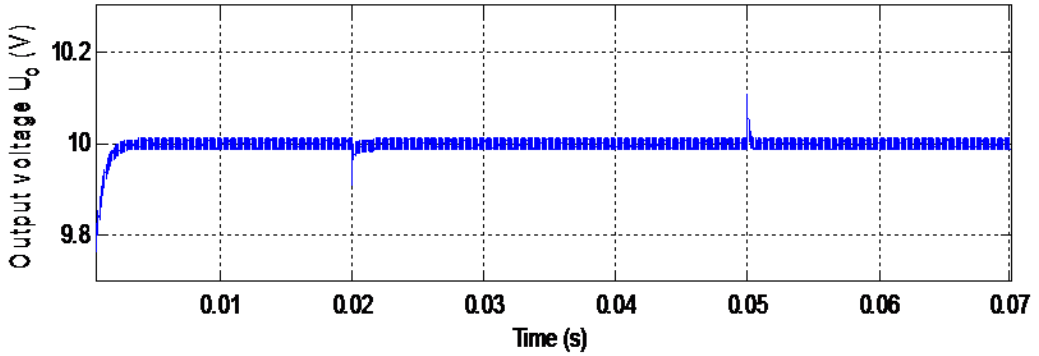


Performance Validation and Simulation

Time-Domain Analysis

The output voltage responses for load disturbances

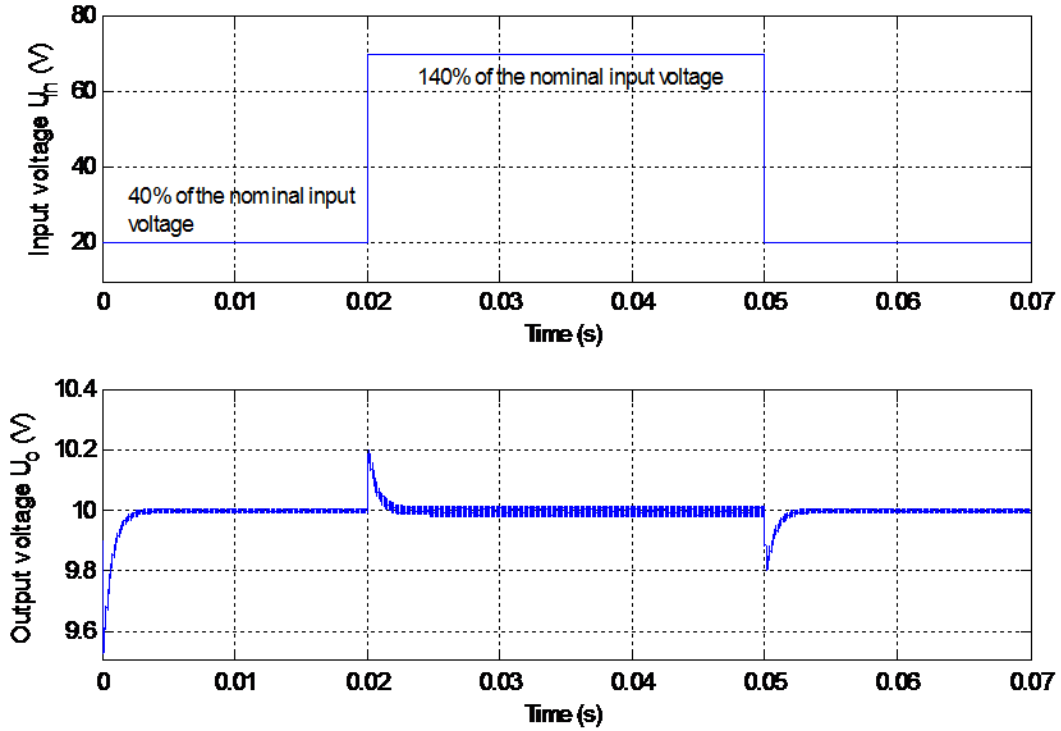




Performance Validation and Simulation

Time-Domain Analysis

The output voltage responses for input disturbances



Conclusions

- The power of averaging small-signal modeling approach in modeling of a dc-dc switching-mode power converters was discussed.
- The resulting wave-forms are averaged and linearized giving models, which are accurate up to half of the switching frequency.
- Small-signal models or transfer functions are used in the dynamical characterization of switched-mode converters.
- A robust control design procedure based on QFT has been applied to switching-mode dc-dc buck converter operating in continuous and discontinues conduction mode.
- The controller and prefilter were designed to meet the frequency domain tracking specifications, robust stability, and disturbance rejection requirements.
- It has been demonstrated that this technique is suitable for application in this case, which presents uncertainties in the parameters.

Conclusions

- The redesign and tradeoffs between the system performance specifications and the controller complexity can easily be done, which provides the designer with more versatile solutions.
- The obtained QFT controller has shown to be effective, and it involves a simple low-order fixed controller.
- The time-domain simulation results show fast recovery of the desired output voltage with zero steady-state error.